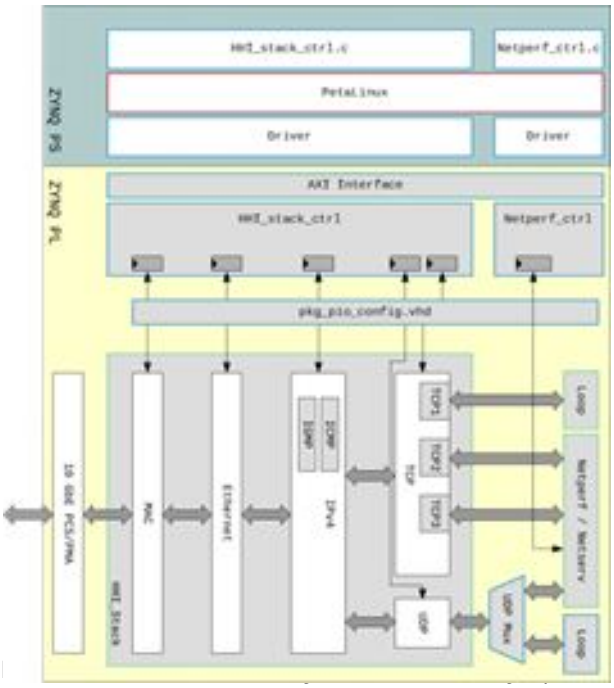
# 10G/25/50/100/200/400G TCP / UDP / IP Solutions for FPGA

MLE markets the industry proven TCP/UDP/IP Network Protocol Acceleration Platform (NPAP) from Fraunhofer HHI. This customizable solution is a high-bandwidth, low-latency communication solution for 1, 10, 25, 40, 50, 100, 200, 400 Ethernet in AMD Ultrascale+ and AMD Versal devices.

## Application Use Cases

- Full TCP/UDP/IP connectivity for FPGAs
- High-speed sensor DAQ: Stream data from FPGA into Network-Attached Storage (NAS)
- High-speed robotics control: Stream data from servers via FPGA into actuators
- High-bandwidth, low-latency automotive ECU-to-ECU connectivity e.g. for SOME/IP
- SmartNIC using TCP/IP “Full Acceleration”
- Hyper-converged computational storage acceleration, for “over-Fabric” NVMe/TCP
- Deterministic low-latency, high-bandwidth alternative to lwIP or Linux on embedded CPU

## System Block Diagram




## Key Features

- Highly modular TCP/UDP/IP Stack implementation for MAC, Ethernet, IPv4, TCP, UDP processing implemented in synthesizable HDL
- IPv4 with ICMP and IGMP
- Bi-directional 128-bit data streams to deliver line rates up to 60 Gbps (depends on FPGA speed)
- Multiple, parallel TCP engines (sockets) for predictable scalable processing
- Network Interface Card (NIC) with optional Bypass and PCIe DMA
- Point-to-point of LAN capable
- Tested for interoperability with TCP/UDP/IP from Linux, Microsoft WIndows, SolarFlare, Mellanox
- User applications for payload processing either in programmable logic or in software via PL/PS datamovers
- Resource analysis for full stack including UDP plus 2 TCP ~30k LUTs, +10k LUTs for each additional TCP engine

## Deliverables

- As IP Core or customized FPGA subsystem
- Single-Project-Use Netlist (or equiv.)
- Multi-Project-Use Source Code
- Customized, integrated turnkey solutions
- Application-specific expert design services

## Contact Information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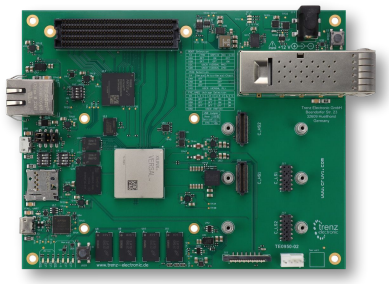
## Exemplary Evaluation Reference Designs (ERD)

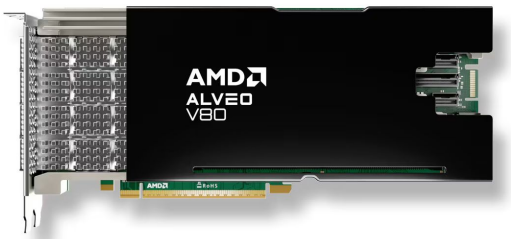
- Full network stack, including low-latency MAC
- TCP/UDP Netperf/Netserv (interops w/ open-source Netperf/Netserv V2.6
- TCP Loopback and UDP Loopback
- Stack control software (for IP addresses, etc)



▲ AMD Versal AI Edge on TE0950 DevKit

## AMD Versal AI Edge on TE0950 DevKit

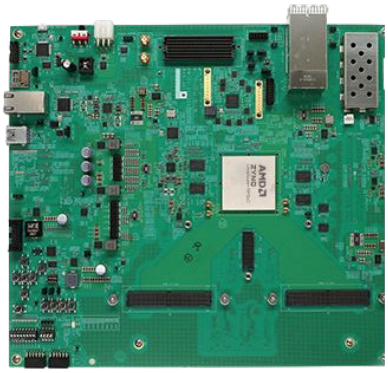
- 10 GigE with 9.8 Gbps linerate
  Integrated with Xilinx 10G/25G Ethernet Subsystem PG210 and GTYP transceivers
- zQSFP for 10 GigE via Twinax or Fibre




▲ AMD Alveo V80 Compute Accelerator Card

## AMD Alveo V80 Compute Accelerator Card

- 10 GigE with 9.8 Gbps linerate
  Integrated with Xilinx 10G/25G Ethernet Subsystem PG210 and GTYP transceivers
- 100 GigE with up to 78 Gbps linerate
  Integrated with Xilinx 100G Ethernet Subsystem PG165 (CMAC)
- QSFP56 for 10/25/40/50 GigE via Twinax or Fibre



▲ Xilinx ZU49DR RFSoC on ZCU216 DevKit

## Xilinx ZU49DR RFSoC ZCU216 Evaluation Kit

- 25 GigE with 24.2 Gbps linerate
  Integrated with Xilinx 10G/25G Ethernet Subsystem PG210 and GTY transceivers
- SFP28 for 10/25 GigE via Twinax or Fibre

## Fraunhofer Heinrich-Hertz-Institute (HHI)

Founded in 1949, the German Fraunhofer-Gesellschaft undertakes applied research of direct utility to private and public enterprise and of wide benefit to society. With a workforce of over 23,000, the Fraunhofer-Gesellschaft is Europe's biggest organization for applied research, and currently operates a total of 67 institutes and research units. The organization's core task is to carry out research of practical utility in close cooperation with its customers from industry and the public sector.

Fraunhofer HHI was founded in 1928 and joined in 2003 the Fraunhofer-Gesellschaft as the "Fraunhofer Institute for Telecommunications, Heinrich-Hertz-Institut„ Today it is the leading research institute for networking and telecommunications technology, "Driving the Gigabit Society" .

## Missing Link Electronics (MLE)

We are a Silicon Valley based technology company with offices in Germany. We are partner to leading electronic device and solution providers and have been enabling key innovators in the automotive, defense, industrial, medical, test & measurement markets with FPGA-based subsystems and systems.

Our mission is to offload CPUs and accelerate software-rich system stacks via so-called Domain-Specific Architectures. To implement this we make heavy use of heterogeneous processing such as FPGAs which we program using C++/C/SystemC as well as VHDL and Verilog HDL.

Our expertise is to "proudly source elsewhere" which means rather than re-inventing the wheel we license (and sublicense) 3rd party IP cores from our growing list of partners and combine this with Open Source Software like Linux to deliver Full System Stacks for FPGA. Today, we offer high-performance (embedded) compute, image-processing, storage and network systems and solutions as well as licensable system stacks for adaptable compute platforms.





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