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| **Day** | 27.02.2019 |
| **Time** | 16:00 - 16:30 |
| **Session/Workshop** | Session 10.2 II |
| **Title** | System-Level Modeling of Heterogeneous Compute Architectures for NVMExpress Protocol Acceleration |
| **Description** | Heterogeneous Compute Architectures embed so-called programmable function accelerators. These accelerators can increase system performance while reducing processing latency and system power. In particular for protocol processing it is quite difficult to know in advance what effects acceleration will have. Therefore, so-called Timed Functional Transaction-Level Models can be used for architecture exploration.<br><br>Using NVMe as the state-of-the-art flash storage protocol as an example we can present a SystemC model to overcome the inefficiency of common CPU centric architectural approaches designed for x86 server architectures in embedded systems. We provide insights in the process of designing the SystemC model, including identifying and characterising the different SoC components needed for performance estimation. By reorganizing SystemC modules we can investigate effects resulting from architectural changes.<br>As a baseline we use the Xillinx Zynq-7000 based ZC706 evaluation system which can easily implement a CPU centric architecture leveraging the Linux Kernel NVMe drivers. Real-world measurements with the ZC706 are used to identify suitable parameters for the SystemC model.<br><br>The presented architectures evaluate the effect of heterogeneous and homogeneous approaches, with respect to data and control paths. We share both the performance estimation and validation measurement. We conclude with a discussion of the lessons learned for architecture exploration based on SystemC models. |
| **Speaker 1** | Cedrik Bock, Missing Link Electronics<br><br>Cedrik Bock got his B.Sc. and M.Sc. degree in Communications and Computer Engineering. He is now a member of the engineering staff at Missing Link Electronics where he is focused on embedded software / hardware Co-development. |