Programming Reconfigurable Devices via FPGA Regions & Device Tree Overlays

A User View Benchmark on a Declarative FPGA Reconfiguration Framework

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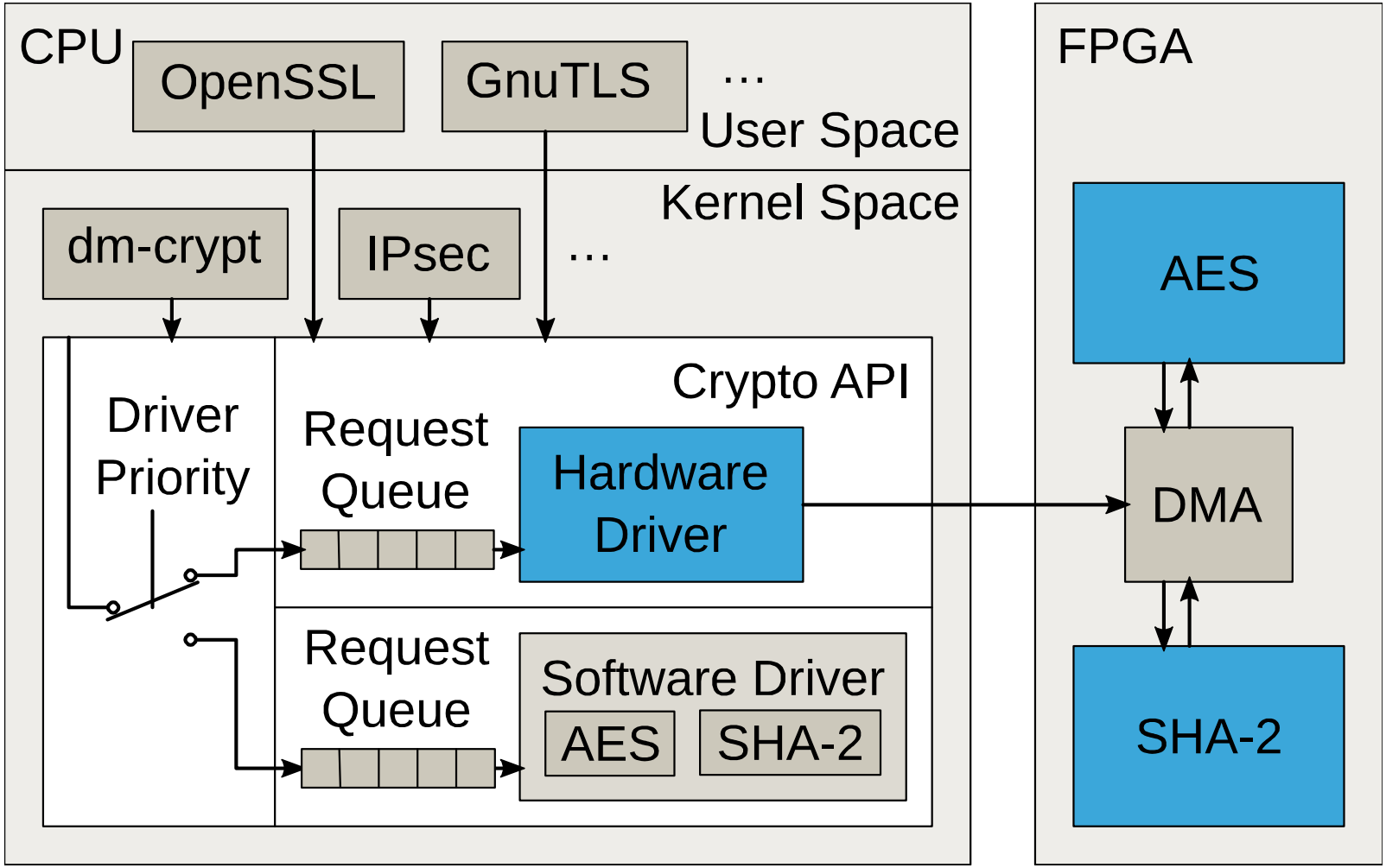
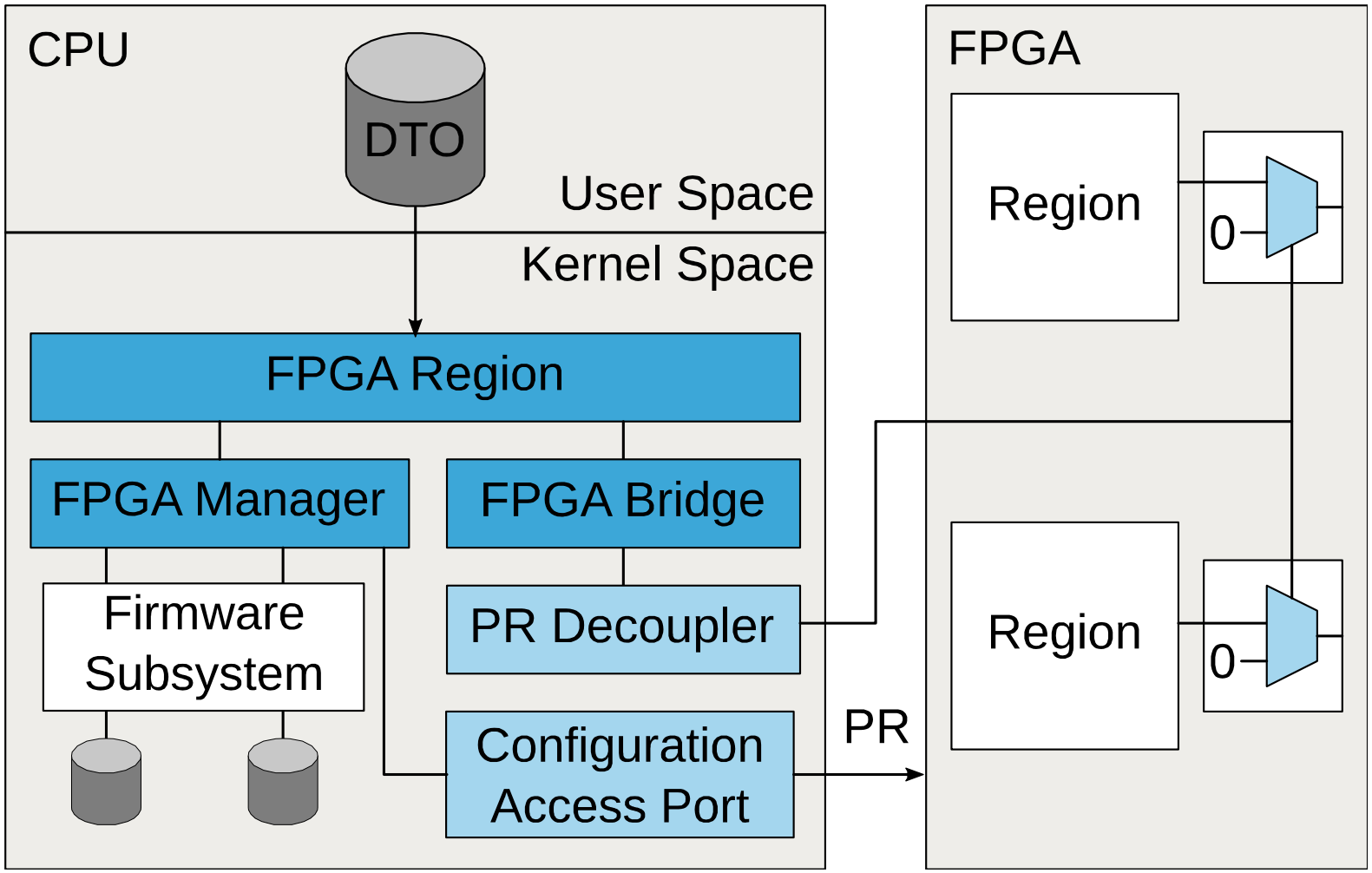
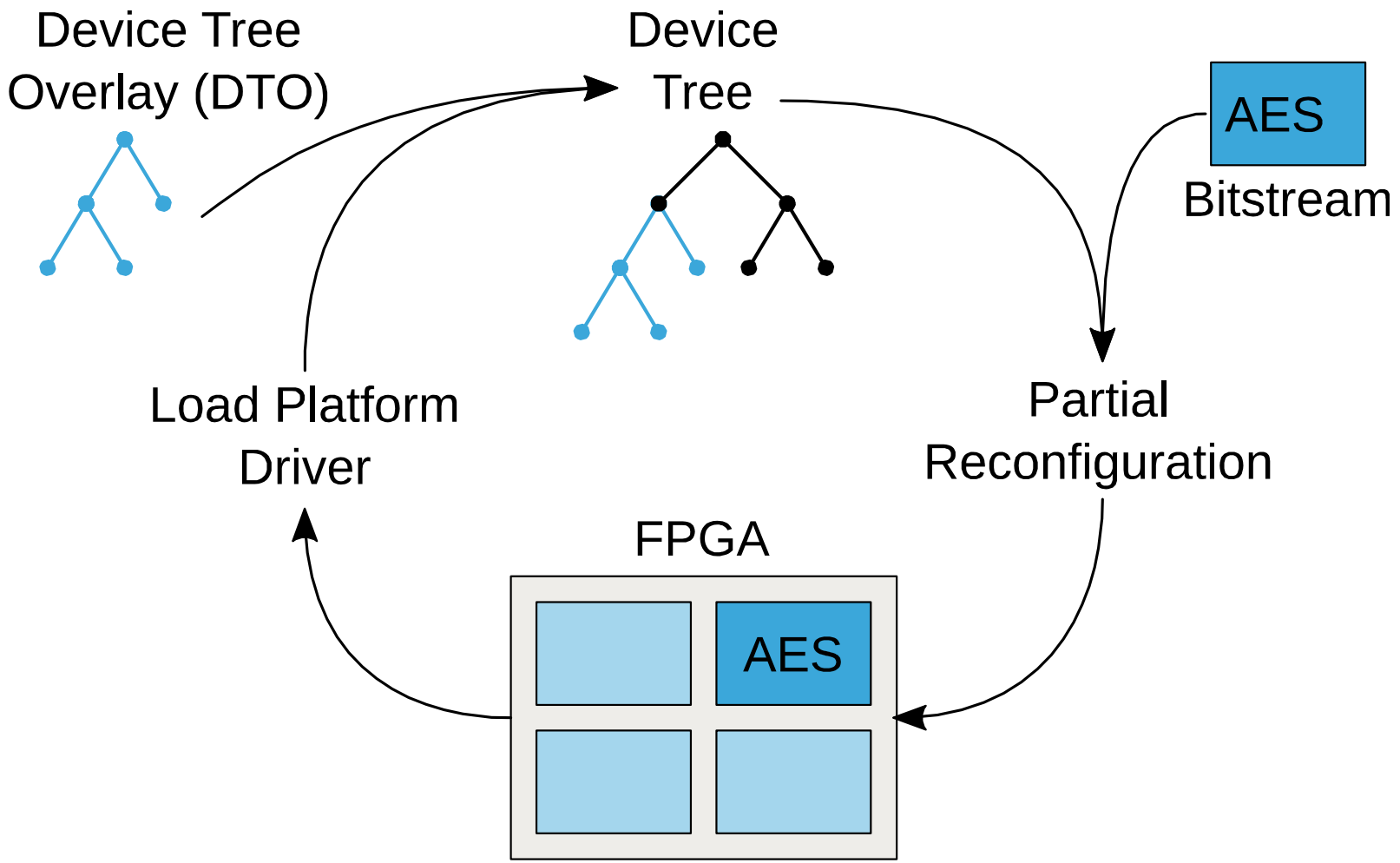
Example System



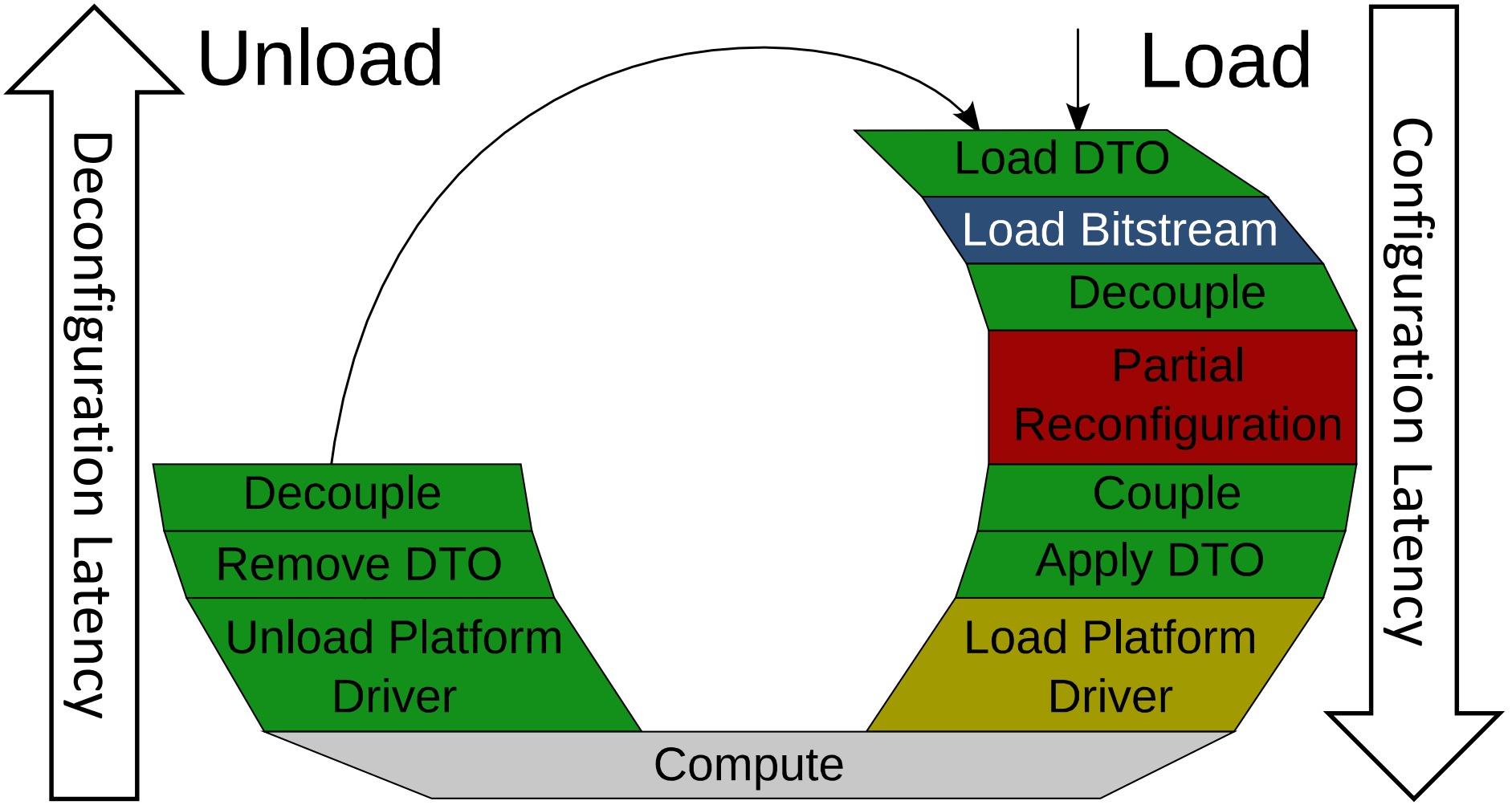
Linux FPGA Framework Architecture



A Declarative FPGA Reconfiguration Framework



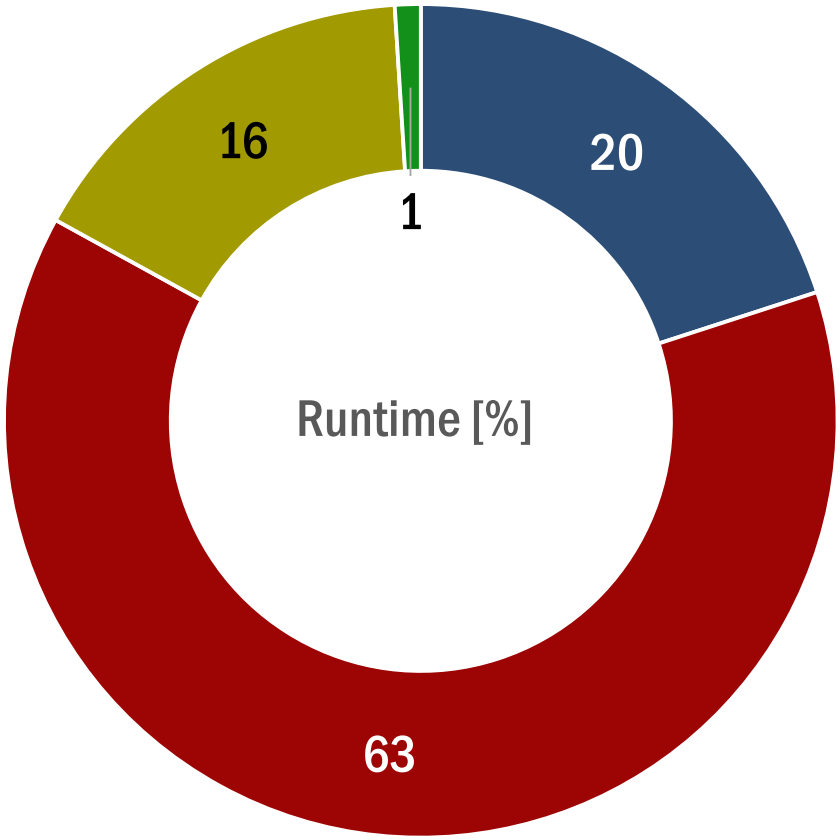
Reconfiguration Performance



Scheduling Latency - Profiling Results

- Measurement of example system (AES accelerator)
- Measured latencies via *ftrace* function entry and exit timestamps

- Bitstream Size: **5.9 MiB**
- Overall latency: **≈135 ms**



Deficiencies / Future Work

Additional Components

- Scheduler / Governor
- User space interface for device tree manipulation
  - Shields & modular embedded systems
  - Reconfigurable systems (FPGA)
- FPGA vendor tools to support DTO generation

Performance Bottlenecks

- Firmware caching
- FPGA reconfiguration interface

  (Scope of FPGA vendors)

Simplifies Reconfigurable Computing on Linux Systems

- Linux DTO & FPGA Framework enables efficient operation of reconfigurable computing systems
  - Supports scheduling time slices in fractions of minutes
  - > 10 s between reconfigurations ≈2 % overhead in our case

- Enables efficient development of heterogeneous systems on MPSoC-FPGAs
  - Reboot free debug and test cycles for fast turnaround times
  - Both static and runtime reconfigurable systems profit

References

1. Moritz Fischer, “FPGA Manager & Device Tree Overlays”, FOSDEM 2016, Brussels, 30-Jan-2016.
2. Alan Tull, “Reprogrammable Hardware under Linux”, Embedded Linux Conference Europe 2015, Dublin, 05-Okt-2015.
3. Pantelis Antoniou, “Transactional Device Tree & Overlays: Making Reconfigurable Hardware Work”, Embedded Linux Conference 2015, San Jose, 23-Mar-2015.