Lorenz Kolb, Missing Link Electronics

Testkonzepte für FPGA/ASIC-Entwicklung nach 50 Jahren Moore’s Law

We are
a Silicon Valley based technology company with offices in Germany. We are partner of leading electronic device and solution providers and have been enabling key innovators in the automotive, industrial, test & measurement markets to build better Embedded Systems, faster.

Our Mission is
To develop and market technology solutions for Embedded Systems Realization via pre-validated IP and expert application support, and to combine off-the-shelf FPGA devices with Open-Source Software for dependable, configurable Embedded System platforms

Our Expertise is
I/O connectivity and acceleration of data communication protocols, additionally opening up FPGA technology for analog applications, and the integration and optimization of Open Source Linux and Android software stacks on modern extensible processing architectures.

Testkonzepte für FPGA/ASIC-Entwicklung nach 50 Jahren Moore's Law

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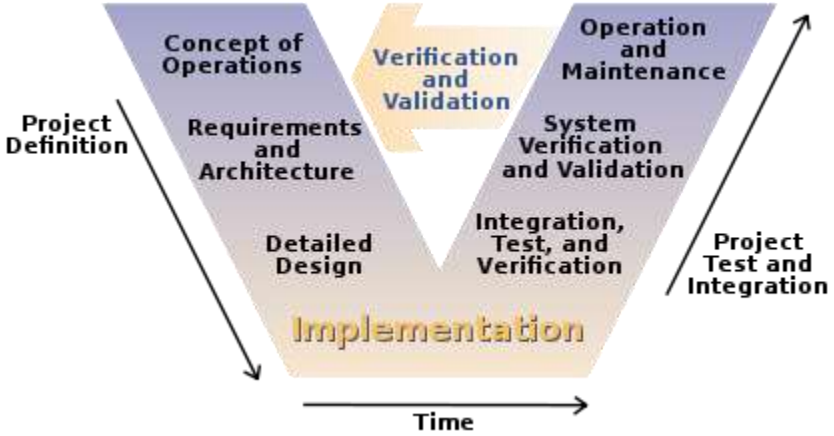
Missing Link Electronics – Lorenz Kolb

- Diplom-Ingenieur Elektrotechnik Universität Ulm, 2008
- Co-Founder Missing Link Electronics
- Expertise
  - Flash Memory Testing
    - UFS
    - PCIe
    - SATA
    - SAS
  - Video Processing
  - Highspeed IO

Testing in Microelectronics has a Different Meaning

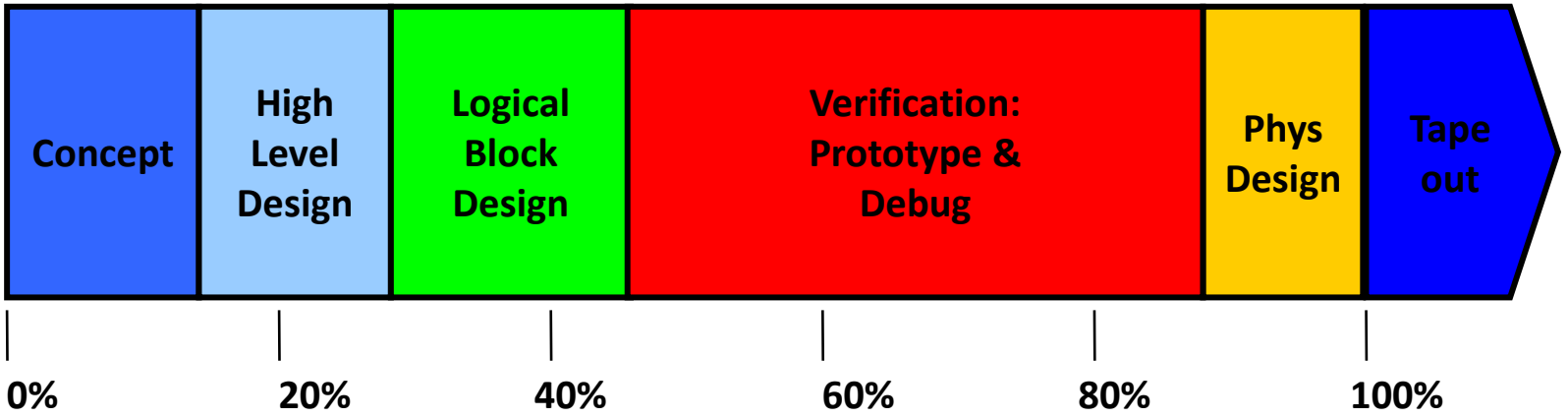


Typical meaning in micro-electronics design (“chip” design) of

- Validation = Checking the correctness of the specification (timing behavior, performance, resource needs, etc).
- Verification = Checking the correctness of the implementation against the specification.
- Test = Checking that the “chip” was manufactured correctly in the fab.

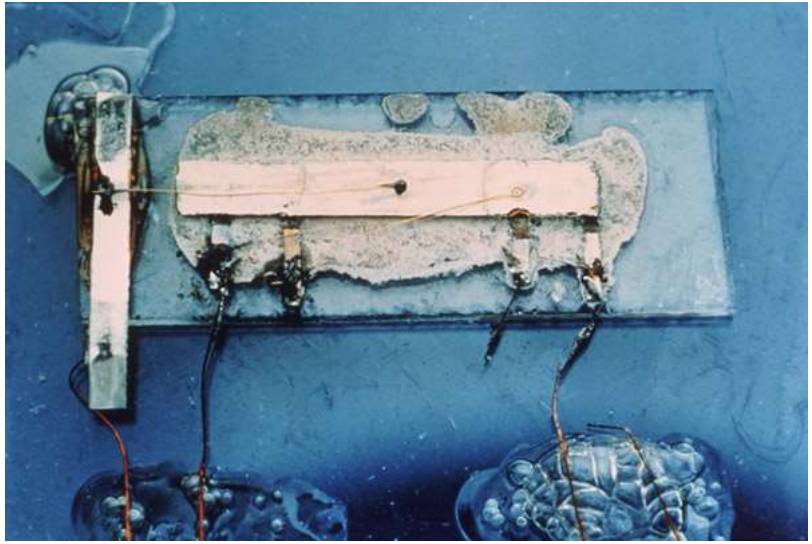
System-on-Chip (SoC) Design Phases

Time spent on different phases in a typical SoC design project
(shown as a linear diagram, alltough SoC is a highly iterative process)

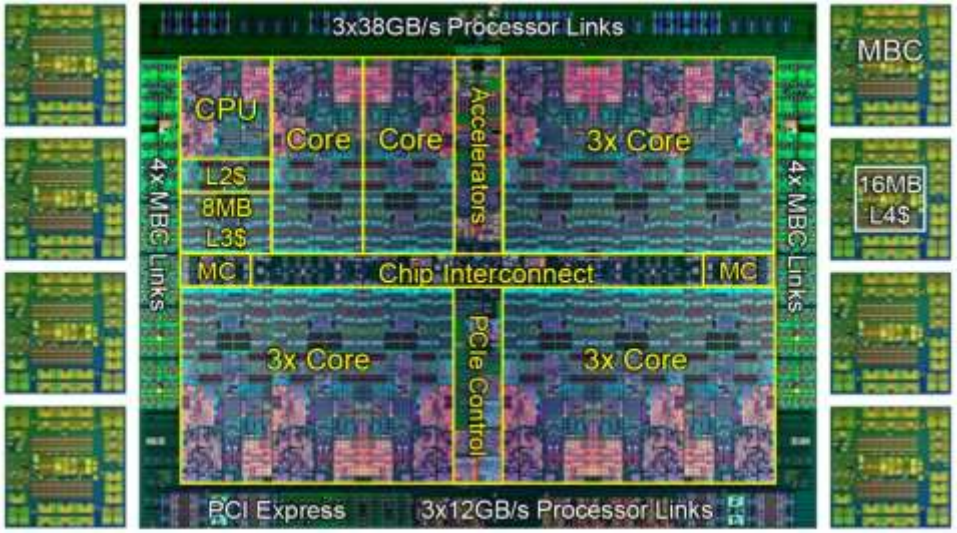


Moore’s Law in Two Pictures

1958 IC - 1 Transistor
(Jack Kilby's first IC)



2015 IC – 4 billion transistors
(IBM Power8 CPU)



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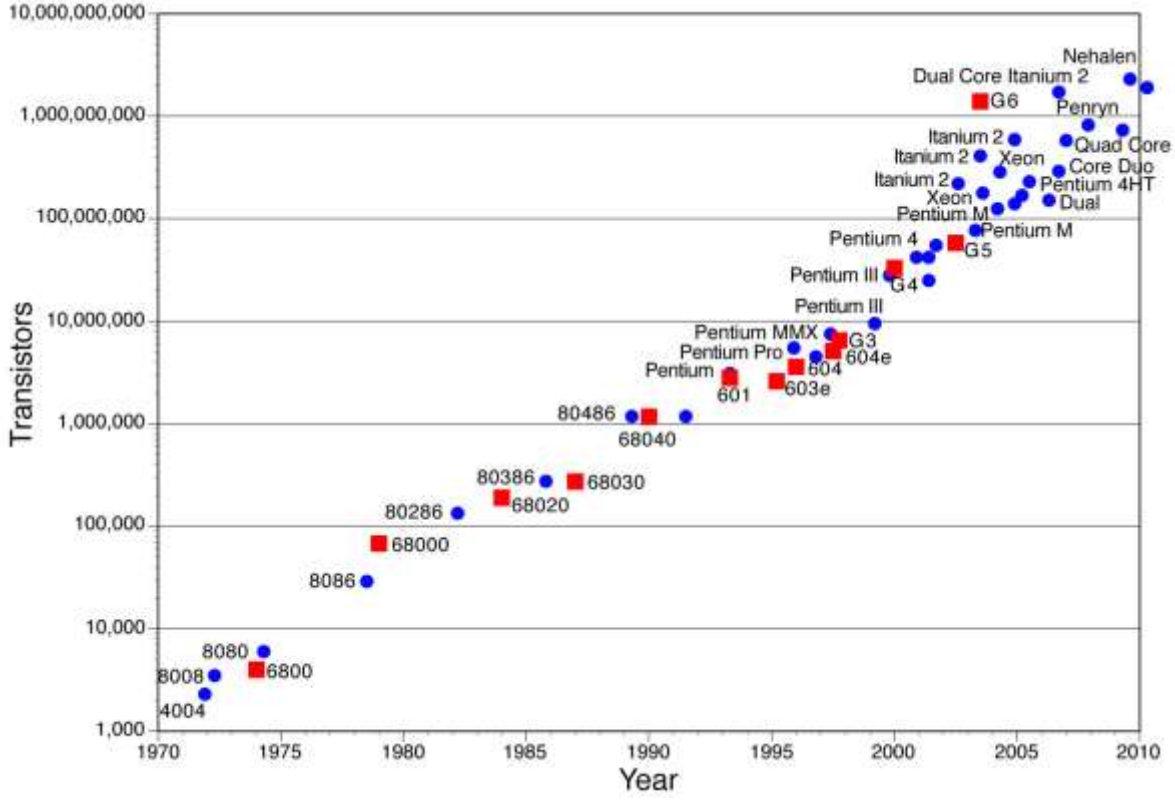
Moore‘s Law – 50 years and counting (1)



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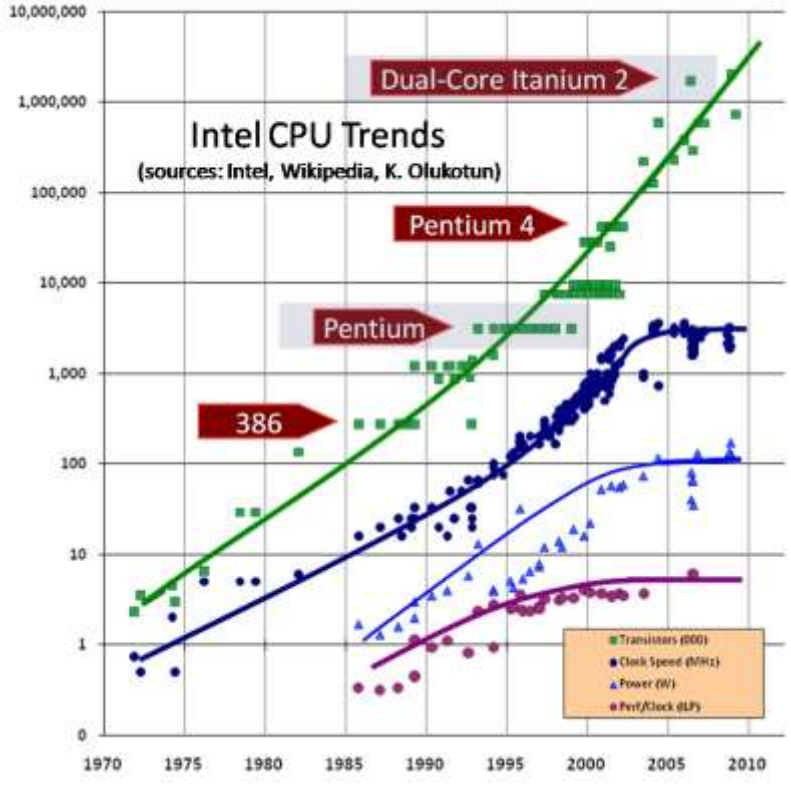
Moore‘s Law – 50 years and counting (2)



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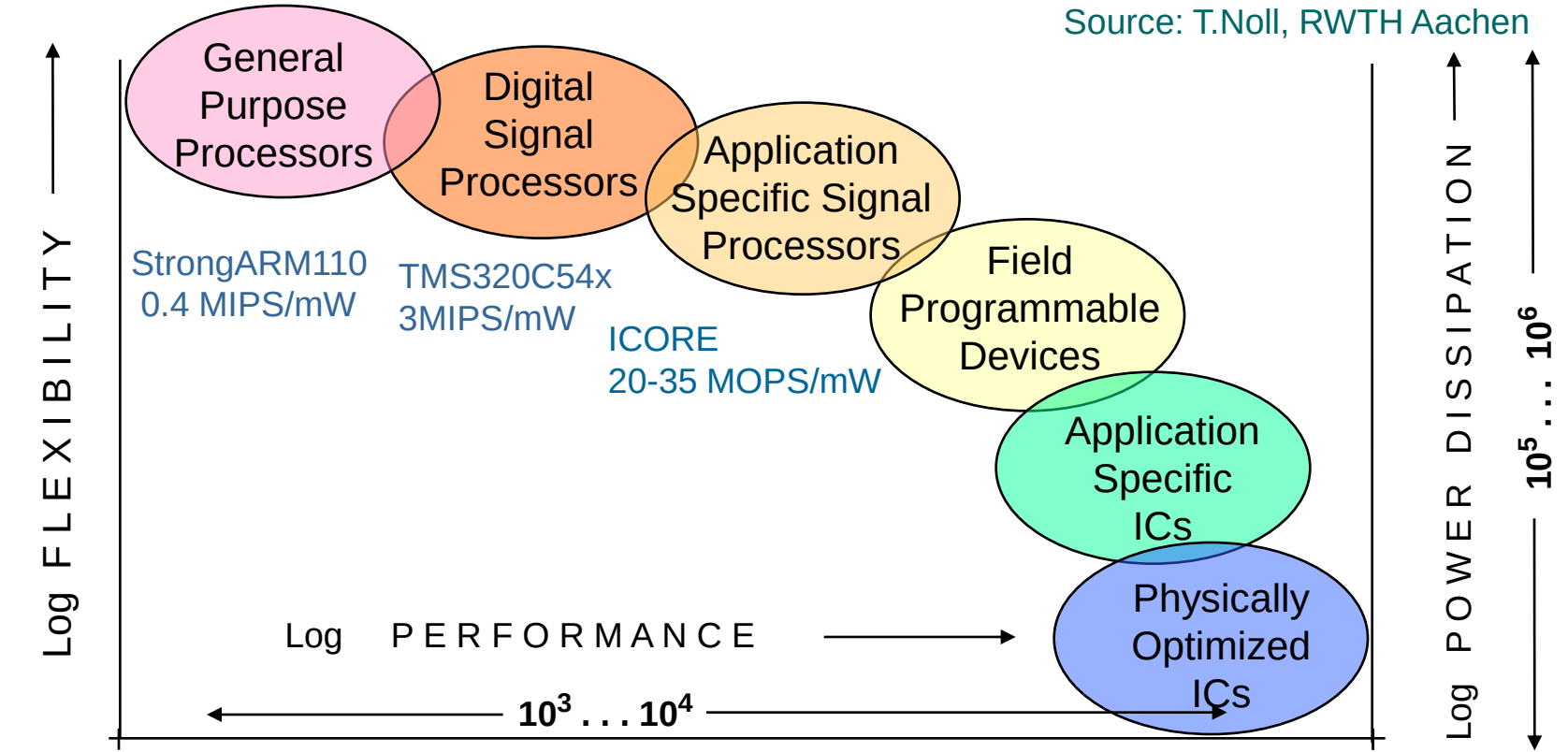
Choices for Implementing Digital Processing



Choices for Implementing Optimized Digital Processing

Application Specific Integrated Circuits (ASIC) or System-on-Chip (SoC)

- Cost of design (NRE > $50m)
- Cost of failure (> $1m per re-spin) drives verification needs (man years)
- Cost of test (CAPEX)

- 1st chip costs $100m , every other chip costs $1

Typically for „Big Boys“ only with large volume (Apple with >100 mio units)

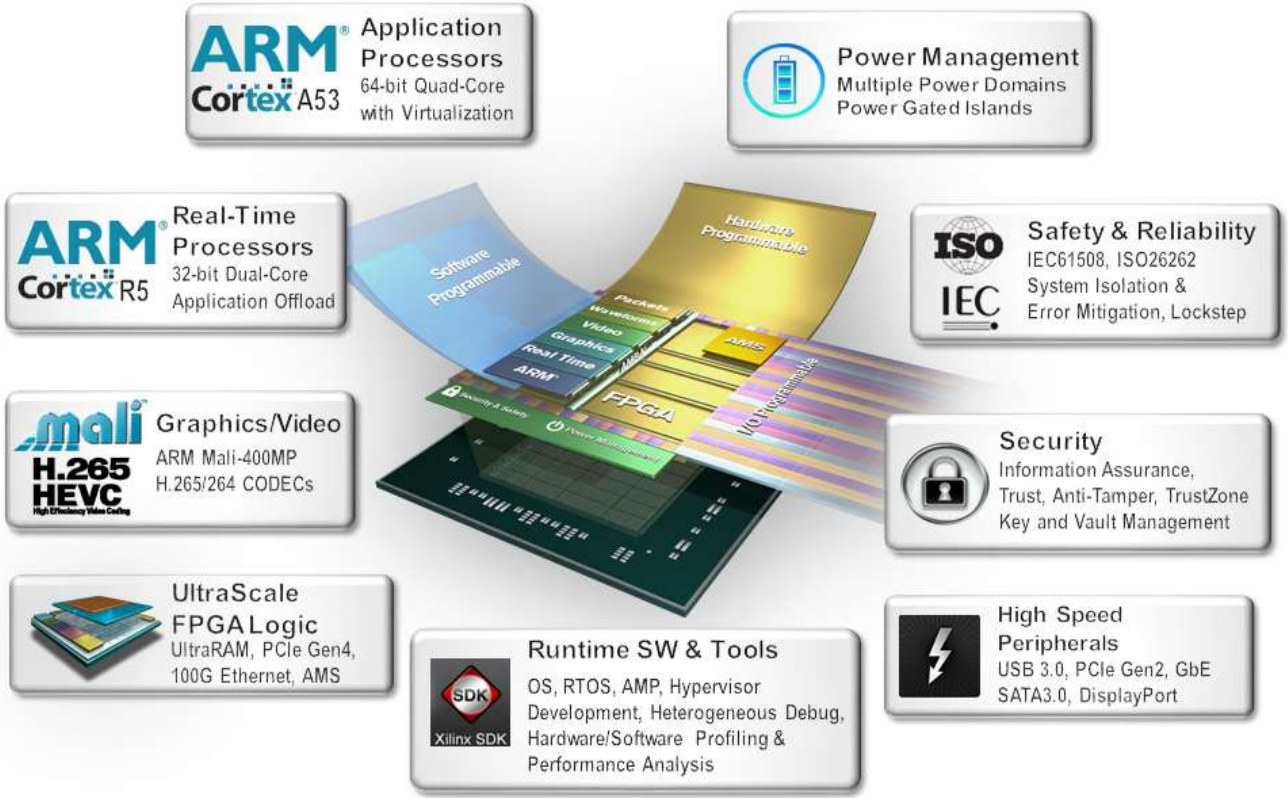
Field-Programmable Gate-Arrays (FPGA)

- Cost of design (few man years)
- Low cost of failure because of reconfigurability in the field relaxes verification needs towards a more software-like debugging approach
- No extra cost of test
- 1st chip costs $100, every other chips costs $100

Cost efficient for small to medium projects in small to large companies.

FPGA as All-Programmable System-on-Chip

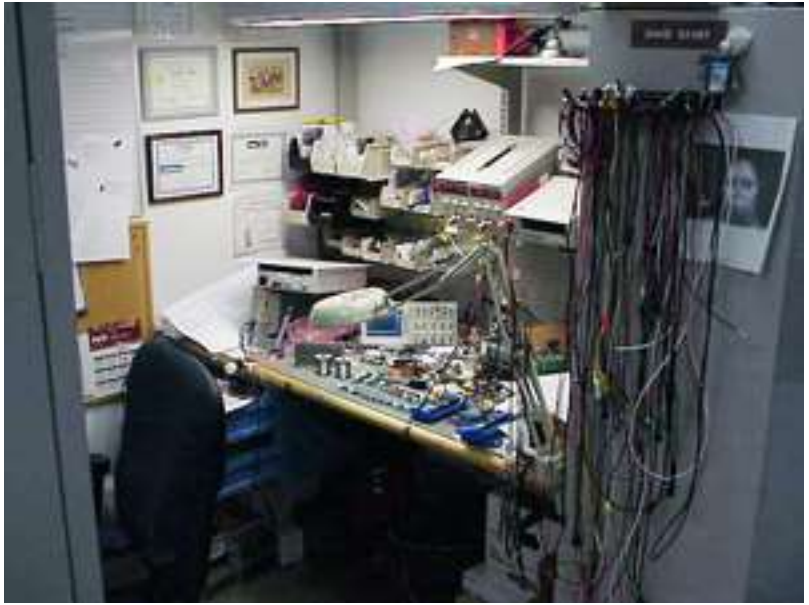
- Programmable I/Os (LVTTL, LVDS, High-Speed SerDes)
- Programmable logic functions (State machines and dataflow)
- Programmable block interconnect (Buses and Network-on-Chip)
- Programmable Fixed-Function Processing (Ethernet MAC, Video Codecs)
- Programmable CPUs (for software processing with or w/o Operating Systems)



Modern FPGAs Enable On-Chip-Debug and Verification

- FPGA is not the DUT!
- FPGA can be the DUT
  plus the TestBench
  plus extra on-chip debug

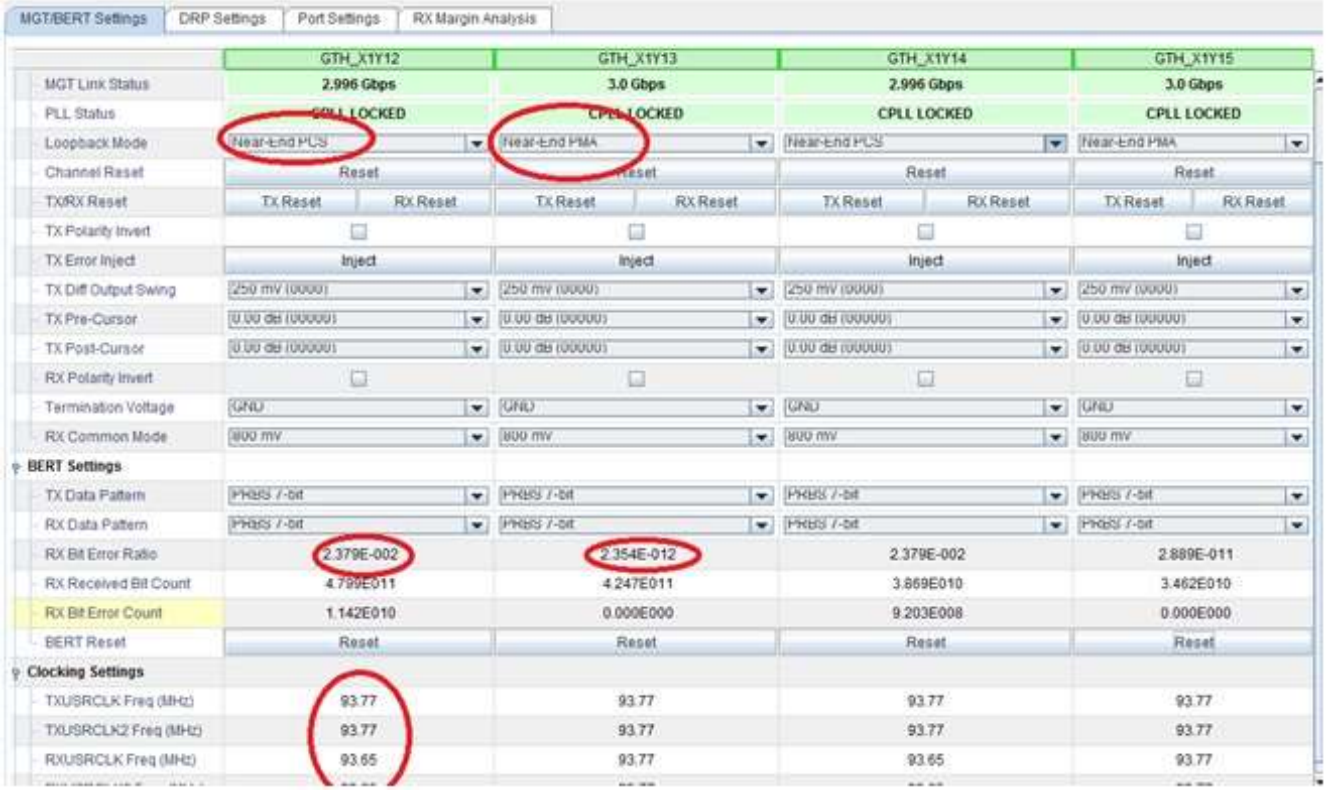
- With on-chip logic analyzers, or on-chip custom debug circuitry, you can analyze and fix your DUT without messy extra hardware setups!



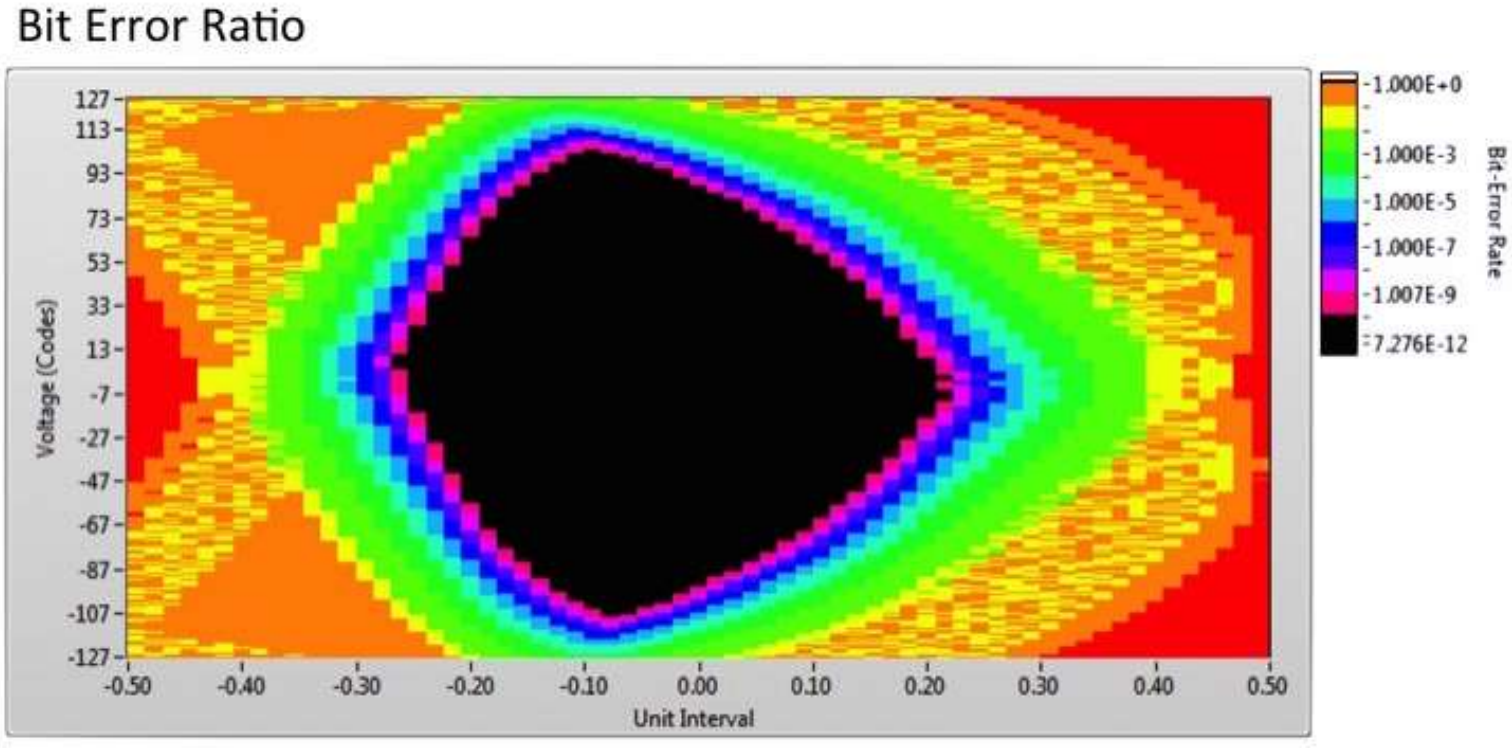
Agile Design and Verification for Modern FPGAs

Abstraction Layer	Example	Design	Verification
Board Level	PCB, chipsets, interfaces, media, etc.	PCB, System Design	Rapid Prototyping In System Debugging
Electronic System Level (ESL)	System-on-Chip	GUI, memeory map, buses, NetworkOnChip	System C models, Bus Functional Models
Functional Blocks	H.264, FEC, AES	In-house or 3rd party IP-Core, High-Level Synthesis	Debug, HighLevel SIM, Co-Simulation
Digital Logic	FSM, control- and dataflow	VHDL, Verilog, SystemVerilog	RTL Simulation, Logic Analyzer
I/O	LVTTL, LVDS, MGT	VHDL, Verilog, Dynamic Reconfiguration Ports	Eye diagrams, Network Analyzer, Oscilloscope

Design and Verification for FPGAs - I/O Programming

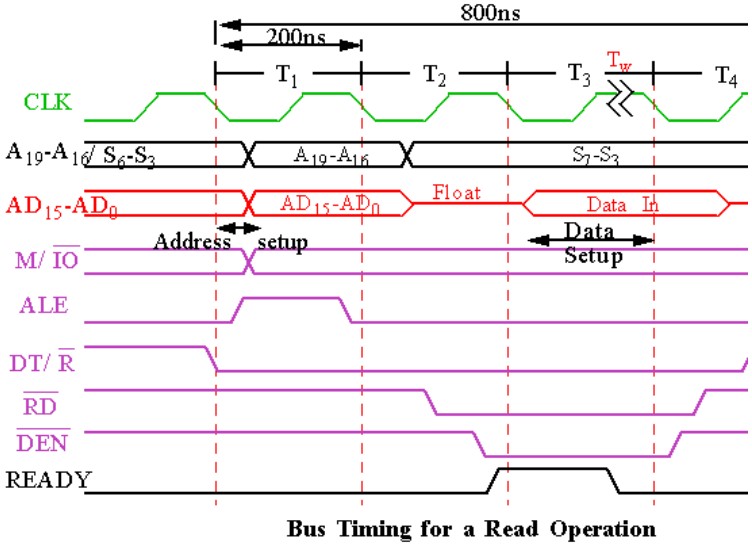


Design and Verification for FPGAs - I/O Verification



Design and Verification for FPGAs – Digital Logic Design

- Typically Hardware Description Languages (HDL) are used such as Verilog and VHDL.
- Designer must describe all 4 dimensions: functionality, structure, parallelism, timing



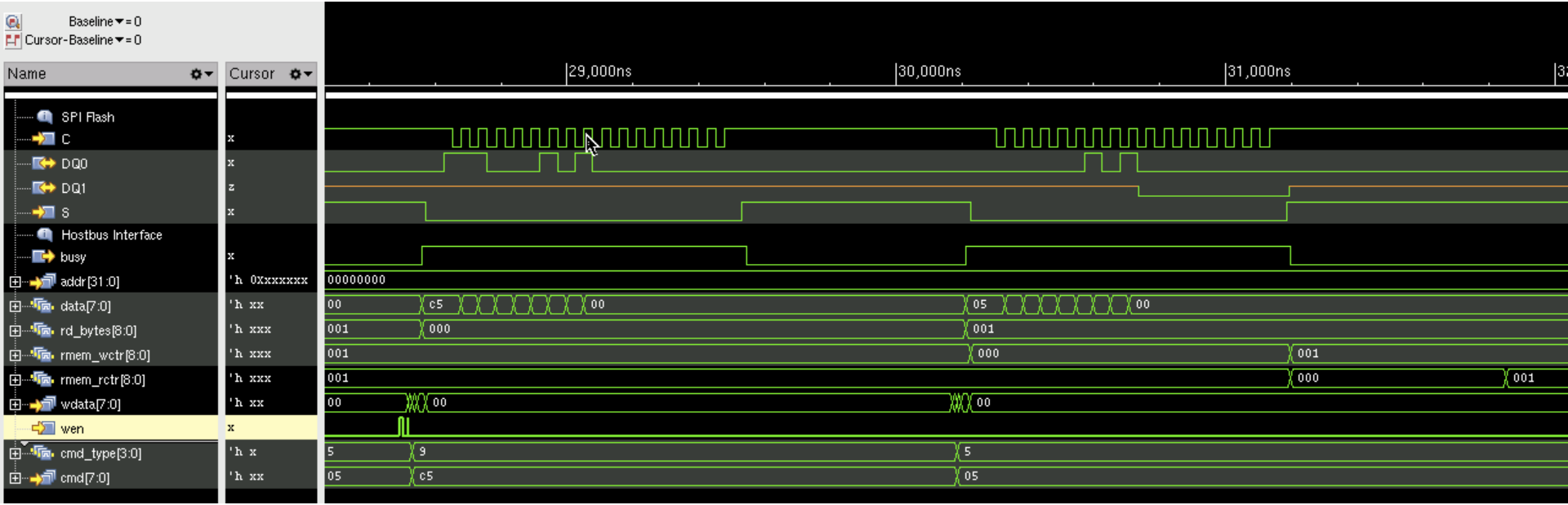
Bus Timing for a Read Operation

```
ENTITY counter IS
  PORT(count_val: OUT integer;
  clk: INOUT BOOLEAN);
END ENTITY counter;

ARCHITECTURE proc OF counter IS
  SIGNAL cnt: integer;
BEGIN
  p: PROCESS
  BEGIN
    WAIT ON clk´event and clk=´1´;
    cnt <= cnt+1;
  END PROCESS p;

  count_val <= cnt;
END ARCHITECTURE proc;
```

Design and Verification for FPGAs – Digital Logic Verification



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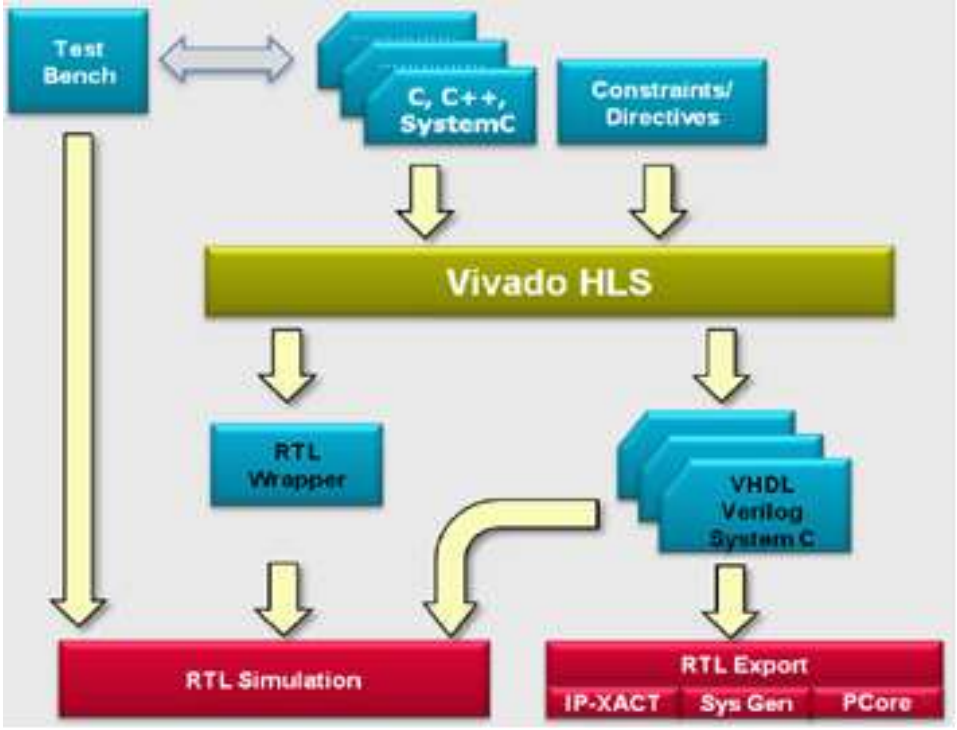
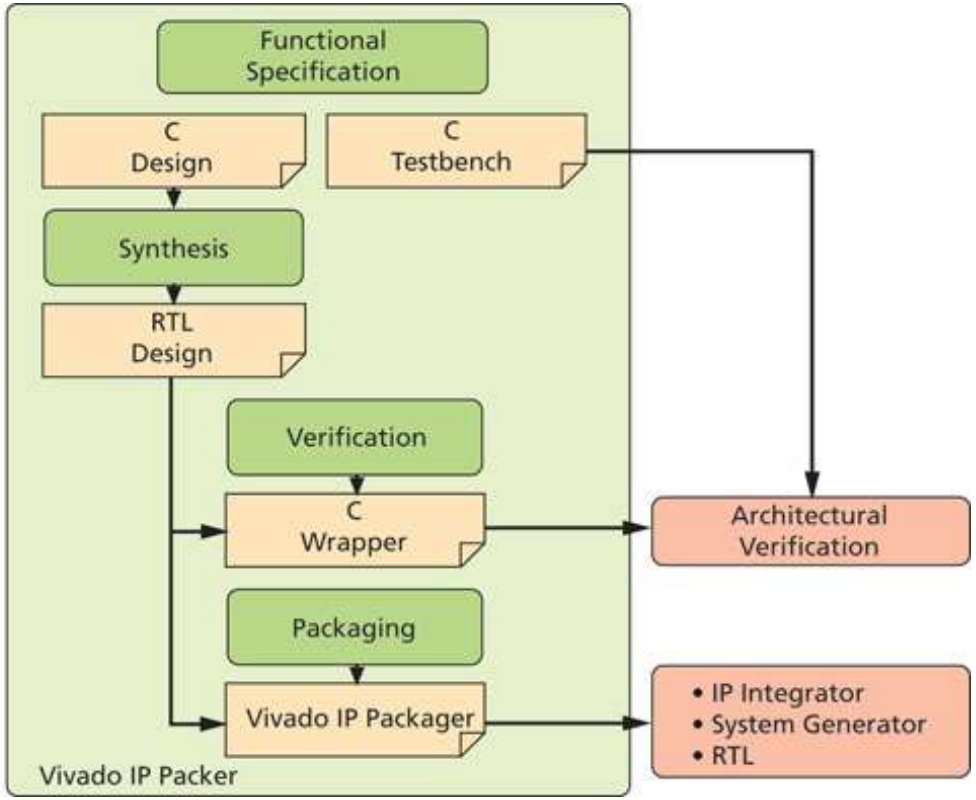
Design and Verification for FPGAs – Functional Block Design

Use of High-Level Synthesis enables functional IP block design in C, C++, SystemC



Design and Verification for FPGAs – Functional Block Verification

- **Starts at C**
  - C
  - C++
  - SystemC
- **Produces RTL**
  - Verilog
  - VHDL
  - SystemC
- **Automates Flow**
  - Verification
  - Implementation



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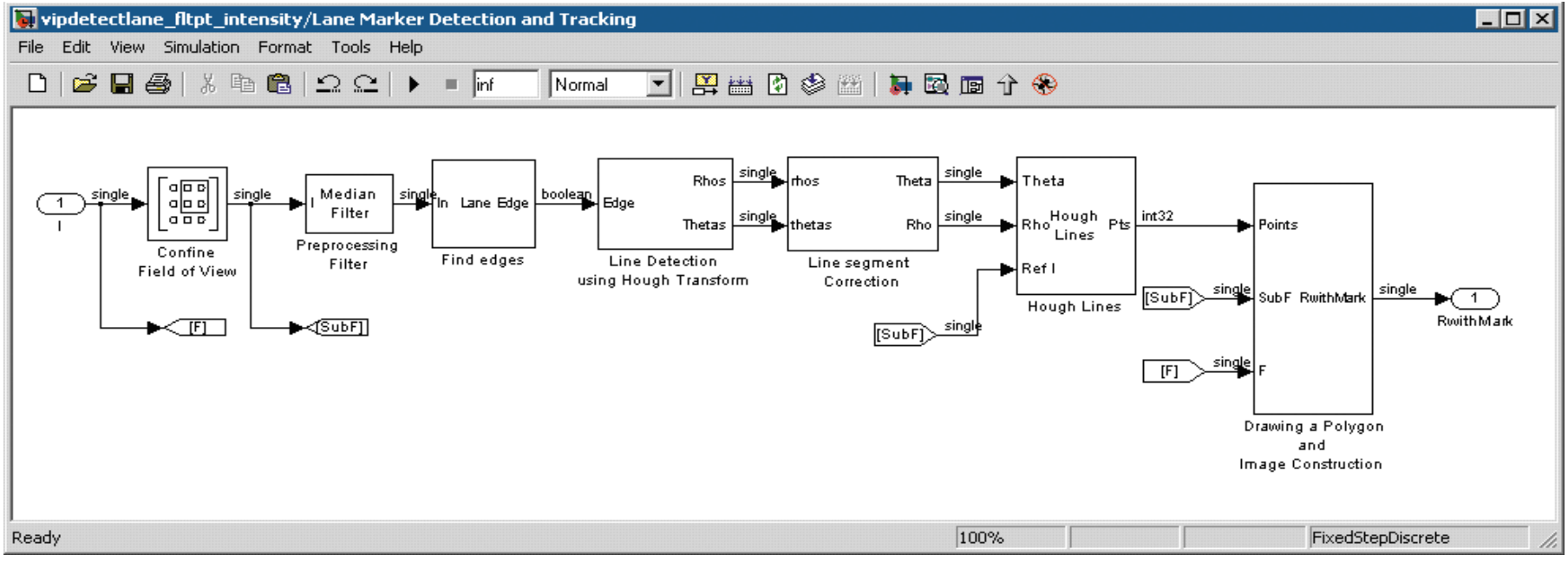
Design and Verification for FPGAs – ESL Design

ESL design is the art of re-using, combining and integrating proper functional blocks.
But: “Don’t design a printer by putting a monitor on top of a copier!”



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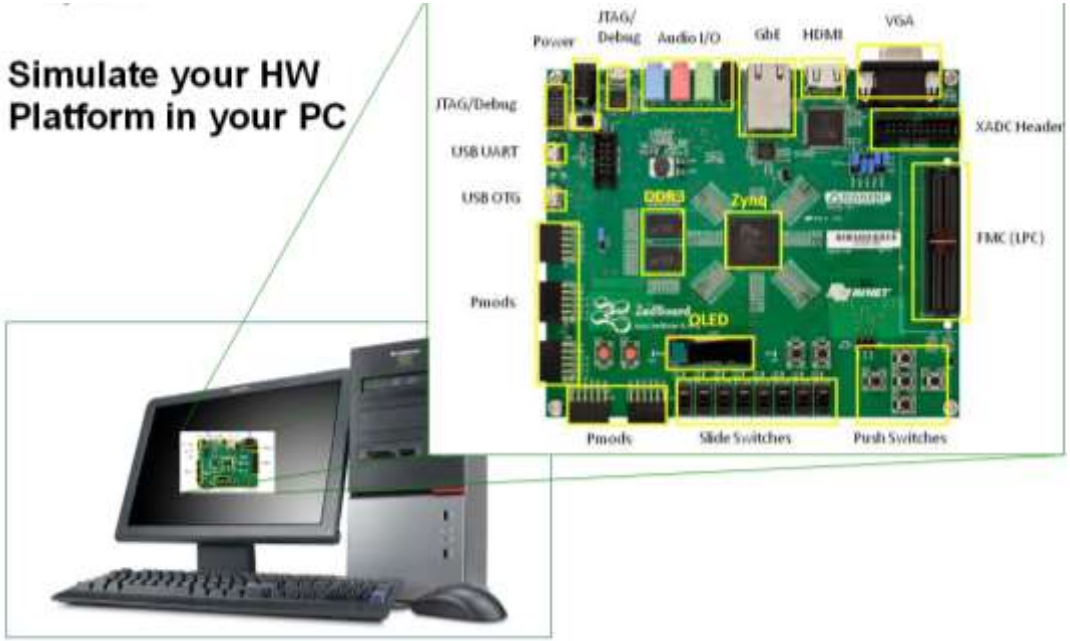
Design and Verification for FPGAs – ESL Verification

Virtual Prototyping allows to run the full system (hardware and software) on your PC



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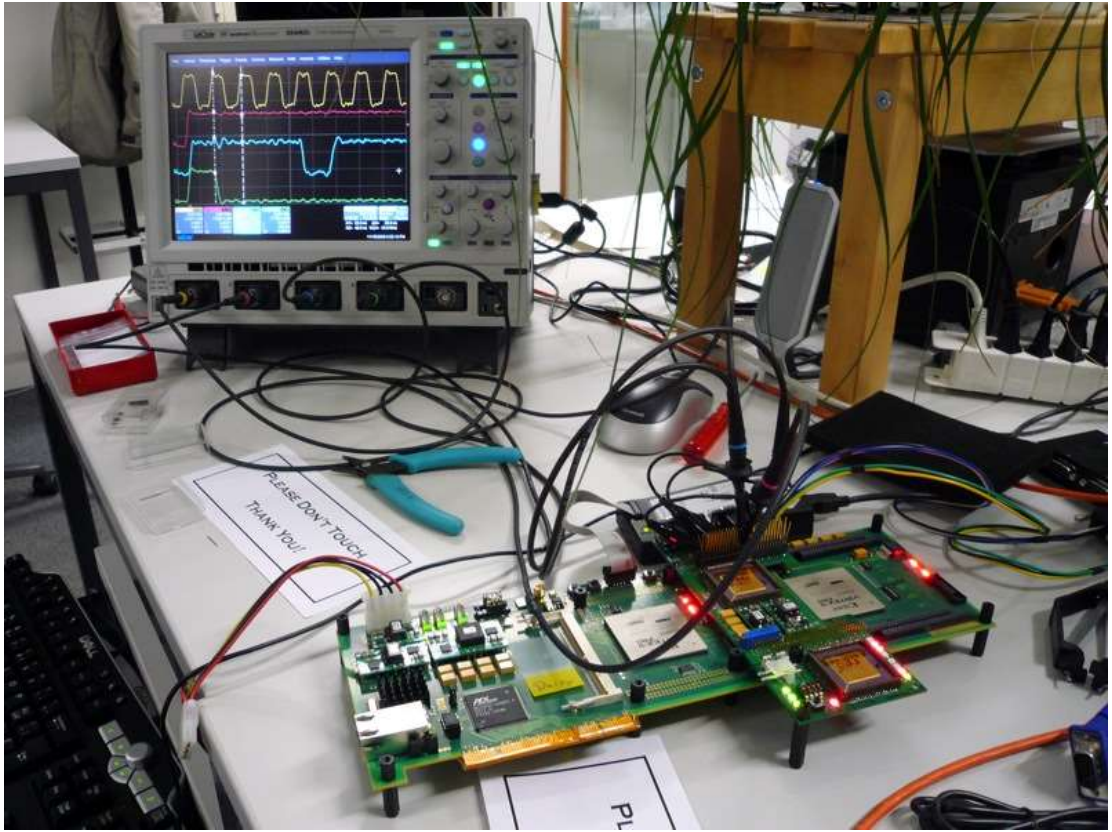
Design and Verification for FPGAs – Board Level Design

Design and Verification for FPGAs – Board Level Verification

- Hardware in the loop
- System in the loop



Conclusion

- Complexity grows exponentially
- Multiple dimensions of testing for HDL
  - Simulation of submodules
  - Co-Simulation with Software
  - In system analysis and debug
  - Board level testing and verification
  - Post production verification and classification
- FPGAs allow post production fixes

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