embedded world 2014
Exhibition & Conference
... it´s a smarter world

”Soft” Analog Solutions for Smart Products

Christian Grumbein
Missing Link Electronics
Neu-Ulm, Germany
Christian.grumbein@mlecorp.com

Dr. Endric Schubert
Missing Link Electronics
Neu-Ulm, Germany
Endric.schubert@mlecorp.com

One branch of Smart Products are embedded systems that can interact with the physical world. Configurability for such Smart Products is a must-have criterion to keep up with fast evolving requirements and deceasing product cycles. Since the real world is analog, also the analog frontend of Smart Products gets into the focus of configurability. This paper will present a bulletproof tested design recipe to utilize digital FPGA I/O pins for analog operations and integrate ”soft” ADC and DAC into modern FPGA. ”Soft” Analog technology can provide reasonable precision at 10-12 bits, sufficient for many analog applications. Most important, it potentially adds another layer of configurability since now a large portion of the analog system setup is moved into the FPGA. This finally enables fast-evolving Smart Products to ensure proper interaction with the physical world and furthermore opens up new analog applications like the 3D acoustic camera.

FPGA; Mixed Signal; Analog; Smart Grid; Smart Camera; Smart Sensor;

I. MOTIVATION

The evolution of embedded systems has taken a new direction with the appearance of what we at Missing Link Electronics (MLE) are calling Smart Products - embedded systems that can control a target electromechanical system. Important features are a rich, interactive user interface, significant local processing capabilities and also the ability to interact with the physical environment through a mix of sensors and actuators.

Challenges for Smart Products are that target electromechanical systems usually evolve slowly over decades, while the smart portions evolve with the speed of internet: new UIs, new sensors and new control algorithms. Thus demand in flexible and configurable interaction to the physical world develops to be must-have criteria for Smart Products.

Digital portions of the Smart Product can comprise of a modern hybrid of an FPGA and an embedded CPU and thus already provide a reasonable grade of configurability. On the other hand, analog portions still tend to decrease design flexibility because of the inability to add, remove or reconfigure the analog channels that interface with the physical world. Nowadays Smart Products sense aspects of their physical environment and return force to it, an aspect that is sometimes also referred to as Cyber-Physical Systems [1]. This process is performed by reading mostly analog sensor data, performing computations, and driving analog actuators and motors.

One or the fundamental motivations are, if and how the configurability of Smart Products can further be enhanced towards analog applications.

II. WHAT IS “SOFT” ANALOG

In order to increase design flexibility also for the analog system setup, a lesser-discussed feature of FPGAs becomes important: The programmable digital I/O capabilities of modern FPGAs. Supporting Low-Voltage Differential Signaling (LVDS) at frequencies of many hundred MHz, FPGA pins have become a viable option to interface with the analog domain [2]. As a result, digital FPGA I/O pins can almost be turned into analog I/O pins [3, 4]. This allows integration of reasonable quality ADC and DAC channels into the FPGA inner-sanctum. The basic idea behind Soft Analog is that the analog system setup (ADC and DAC) becomes configurable.

Configurability in this case applies to fundamental analog parameters like the sample rate, cut-off frequency or gain and offset compensation. And usually, precisions at 10 to 12 bit and sample rates at a few hundred kSPS are classified as reasonable quality, because this is considered to be sufficient for a wide range of analog applications.

Besides the obvious increase in design flexibility (add, remove or configure analog channels), it also opens up simultaneous and time-synchronous sampling of multi-channel systems. The number of analog channels is only limited by the FPGA device pin count and the FPGA logic elements, resulting in potentially dozens of analog inputs and outputs for modern FPGA devices. On the other hand, the PCB footprint and BOM of the overall system can be effectively reduced, since there are no any active peripheral ADC and DAC ICs required. This also allows moving powerful signal processing capabilities closer to the analog source, or sink.

Applications for Soft Analog in Smart Products range from flexible data acquisition and monitoring systems, sensor networks with many inputs, voltage-based actuator control and

DC motor control, control systems, audio applications, to risk reduction of parts obsolescence. This paper will pitch on specific applications: differential measuring, time-synchronous sampling, DC motor control and 3D acoustic cameras.

III. Design Principles for "soft" ADC and DAC

To design and integrate reasonable quality "soft" ADC or DAC for FPGA-based Smart Products, there is a bulletproof tested design recipe that basically comprises of three main ingredients:

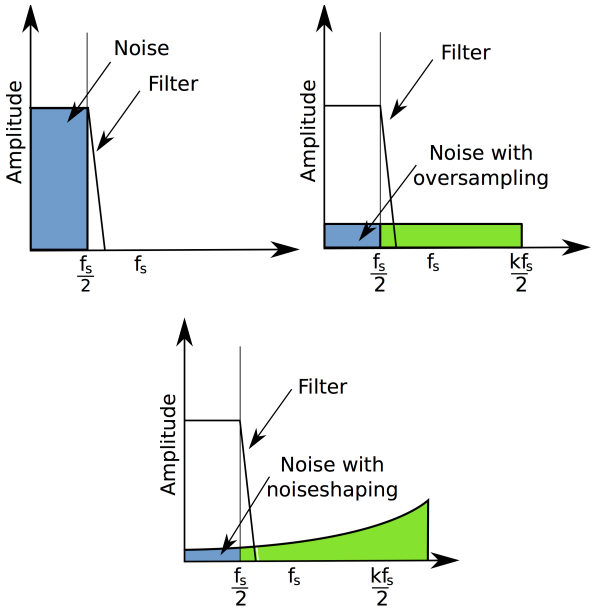

Figure 1

First, it is important to properly qualify the LVDS pins by applying performing extensive low-level simulation modeling [5]. Obviously, the "analog" behavior of an LVDS pin such as hysteresis, finite amplitude decision time or meta-stability cannot be ignored in this case.

Second, a well-integrated digital filter cascade is mandatory for proper configuration and optimization to- wards the desired quality measures. For an ADC implementation, this may comprise of decimation and additional low-pass filtering [3].

Third and finally there needs to be some type of converter implemented. Delta-Sigma modulation (DSM) is a modern approach for converting between analog and digital data, and can be applied to both analog-to- digital converters (ADCs) and digital-to-analog converters (DACs) [5]. There have been many approaches to converting an analog signal into a digital signal over the years. But with the increasing speed and density of digital circuits and the modern preference to use as much digital and as little analog circuitry as possible, DSM techniques have come to dominate the field. DSM provides an inherent feature called Noise Shaping that - on top of basic oversampling - allows to furthermore reducing the user band noise [6]. These effects can be seen in Fig. 1.

Noise Shaping can enable even 1st order DSM implementations to reach Signal-to-Noise ratios above 60dB.

Applying the design recipe as described one can end up with a very compact soft ADC or DAC implemen- tation that provides 10-12 bit precision. Fig. 2 shows an implementation example for a soft ADC. While most of the implementation is in digital logic, only a small portion remains in analog circuitry - a passive-only low pass filter.

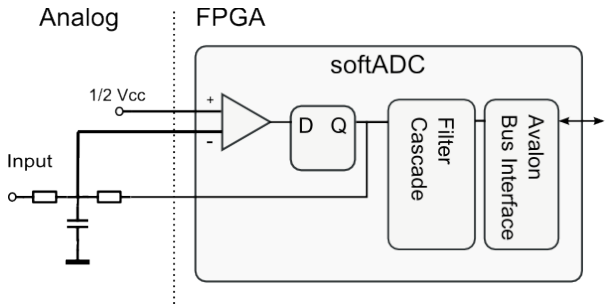

Figure 2

However, the key to assure precision and stability is obtaining a proper parameter set for the DSM. The parameter space addresses the low-pass time constant and the internal DSM sample frequency, which determines the oversampling rate. Fig. 3 shows implementation results for handling these parameters well and also applying optimized post-processing decimation and low pass filtering.

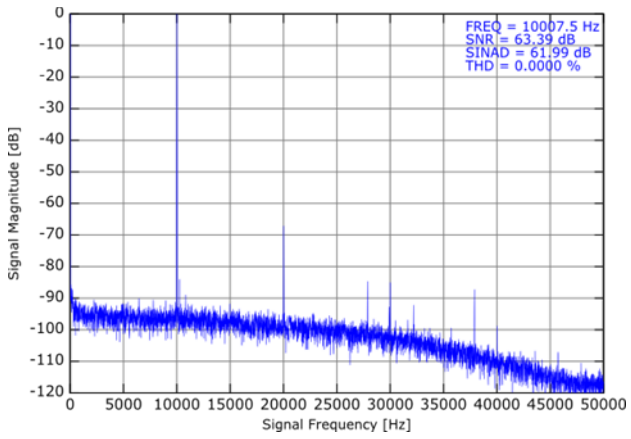

Figure 3

As a result, such comparably small implementations can enable Smart Products for reliable and precise analog operations. Some of the exciting applications will be presented in the following chapter.

IV. Applications

This chapter provides brief introductions into some application examples for Soft Analog in Smart Products.

A. 3D Microphone Array

This application makes use of Advantages, the FPGA integrated ADC has over the commonly used discrete ADC. One of the Advantages used here are the synchronous sampling of multiple ADC Channels, which means, that the Samples of multiple channels are acquired at the same time. This feature makes a straightforward implementation of the 3D Microphone array possible, because the Algorithm does not have to account

for the different sampling times of the Microphones. A schematic of this can be seen in Fig. 4. It shows how the different ADC channels which each connect to a Microphone are filtered and then processed in the Algorithm Block which calculates the positional Data from the input delays and the distribution of the Microphones.

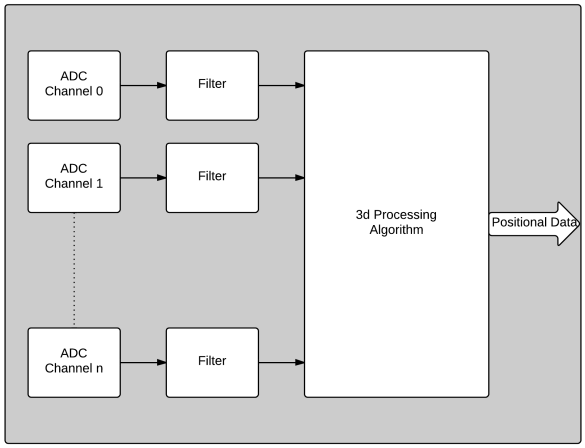

Figure 4

This data can then be used to amplify specific Sources and to dampen noise, or to get an image of the surrounding.

B. FPGA-based Brushless DC Motor Control

This chapter shows the actual implementation of the Delta Sigma ADC, as well as a possible implementation, using the ADC channels to control a BLDC motor. Fig 5 shows the implementation on an FPGA including the passive external circuitry. The difference to the previous implementation is the use of a low-pass and a decimation filter to obtain results compatible to an FPGA-based micro-controller. For our

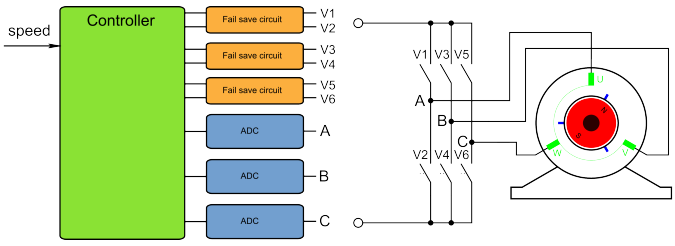

Figure 5

Exemplary implementation we have used the NIOS-II CPU [8] which is available as a soft IP core and can be integrated inside the FPGA plus extra peripherals to form a customizable micro-controller. For the low-pass filter, a resource-efficient moving average filter was chosen, as the normally used CIC filter is not resource-efficient at high oversampling ratios. This ADC was inserted as a soft IP core into the FPGA design. The brush-less controller consists of different modules as shown in Fig. 5. The motor control is done using 3 output modules with a shoot-through prevention each of which connects to the three phases H-bridge that drives the motor. Three Delta-Sigma ADC channels with specialized protection circuits sample the back-EMF the corresponding back-EMF from the motor. From this data, the position of the motor is extrapolated. Connected to these input and output modules is the actual control module which calculates from the back-EMF, the current outputs and the desired speed of the motor the next output of the H-bridge. This modular design also makes the controller adaptable to different motor types and sizes.

CONCLUSION

Configurability for Smart Products is a must-have criterion to keep up with fast evolving requirements and deceasing product cycles. Since the real world is analog, also the analog frontend of Smart Products gets into the focus of configurability. This paper has presented a bulletproof tested recipe to utilize digital FPGA I/O pins for analog operations and integrate soft ADC and DAC into modern FPGA. ”Soft” Analog technology can provide reasonable precision at 10-12 bits, sufficient for many analog applications. Most important, it potentially adds another layer of configurability since now a large portion of the analog system setup is moved into the FPGA. This finally enables fast-evolving Smart Products to ensure proper interaction with the physical world and furthermore opens up new analog applications like the 3D acoustic camera.

[1] P. Marwedel, “Embedded and cyber-physical systems in a nutshell,” DAC.COM Knowledge Center Article, 2010.

[2] F. Sousa, V. Mauer, N. Duarte, R. Jasinski, and V. Pedroni, “Taking advantage of lvds input buffers to implement sigma-delta a/d converters in fpgas,” in Circuits and Systems, 2004. ISCAS ’04. Proceedings of the 2004 International Symposium on, vol. 1, may 2004, pp. I–1088–91 Vol.1.

[3] MLE Technical Brief 20110419, Integrated ADC for Altera Cyclone-IV Devices, 2011.

[4] MLE Technical Brief 20110426, Integrated DAC for Altera Cyclone-IV Devices, 2011.

[5] P. Aziz, H. Sorensen, and J. vn der Spiegel, “An overview of sigma-delta converters,” Signal Processing Magazine, IEEE, vol. 13, no. 1, pp. 61 –84, jan 1996.

[6] P. Aziz, H. Sorensen, and J. vn der Spiegel, “An overview of sigma-delta converters,” Signal Processing Magazine, IEEE, vol. 13, no. 1, pp. 61 –84, jan 1996.

[7] R. Schreier and G. Temes, Understanding Delta-Sigma Data Converters. Wiley, 2004.

[8] R. Schreier and G. Temes, Understanding Delta-Sigma Data Converters. Wiley, 2004.