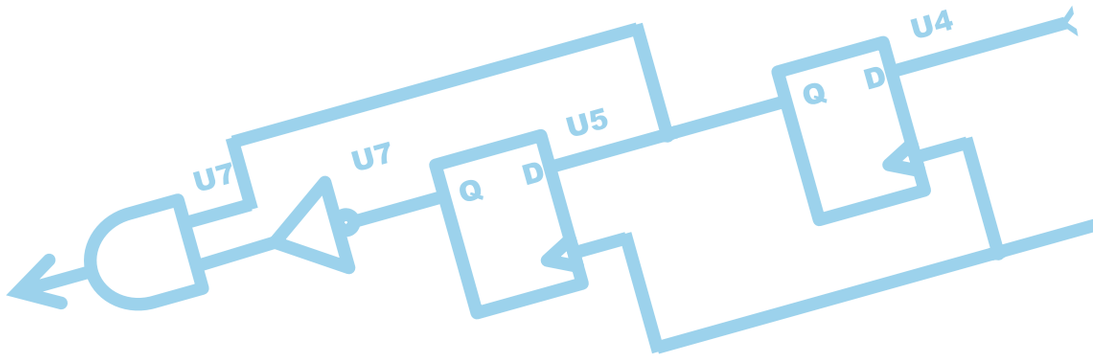


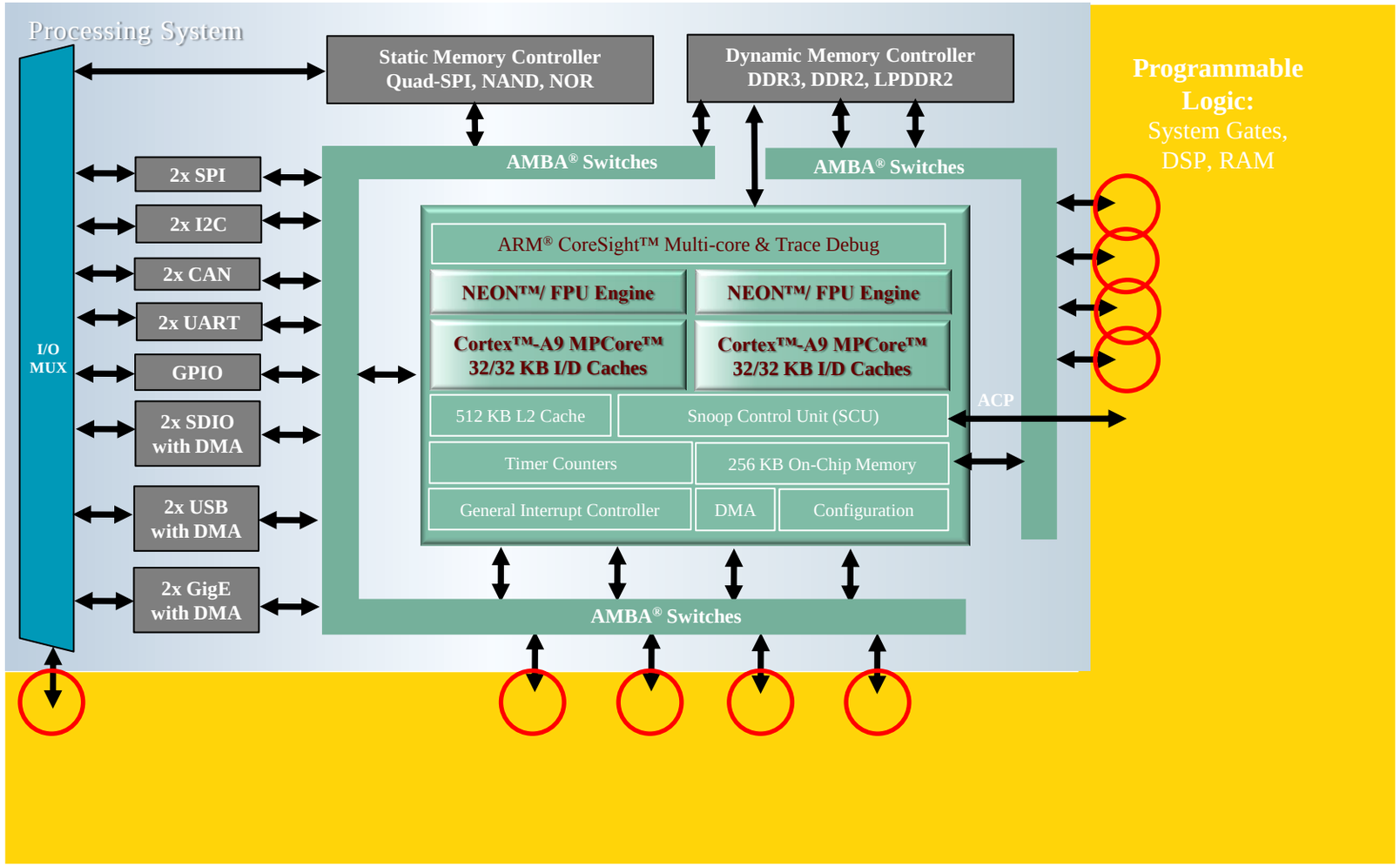
Zynq-SoCs mit busfunktionalen Modellen debuggen

Endric Schubert, Missing Link Electronics

cadence™ XILINX® SILICA™ An Avnet Company

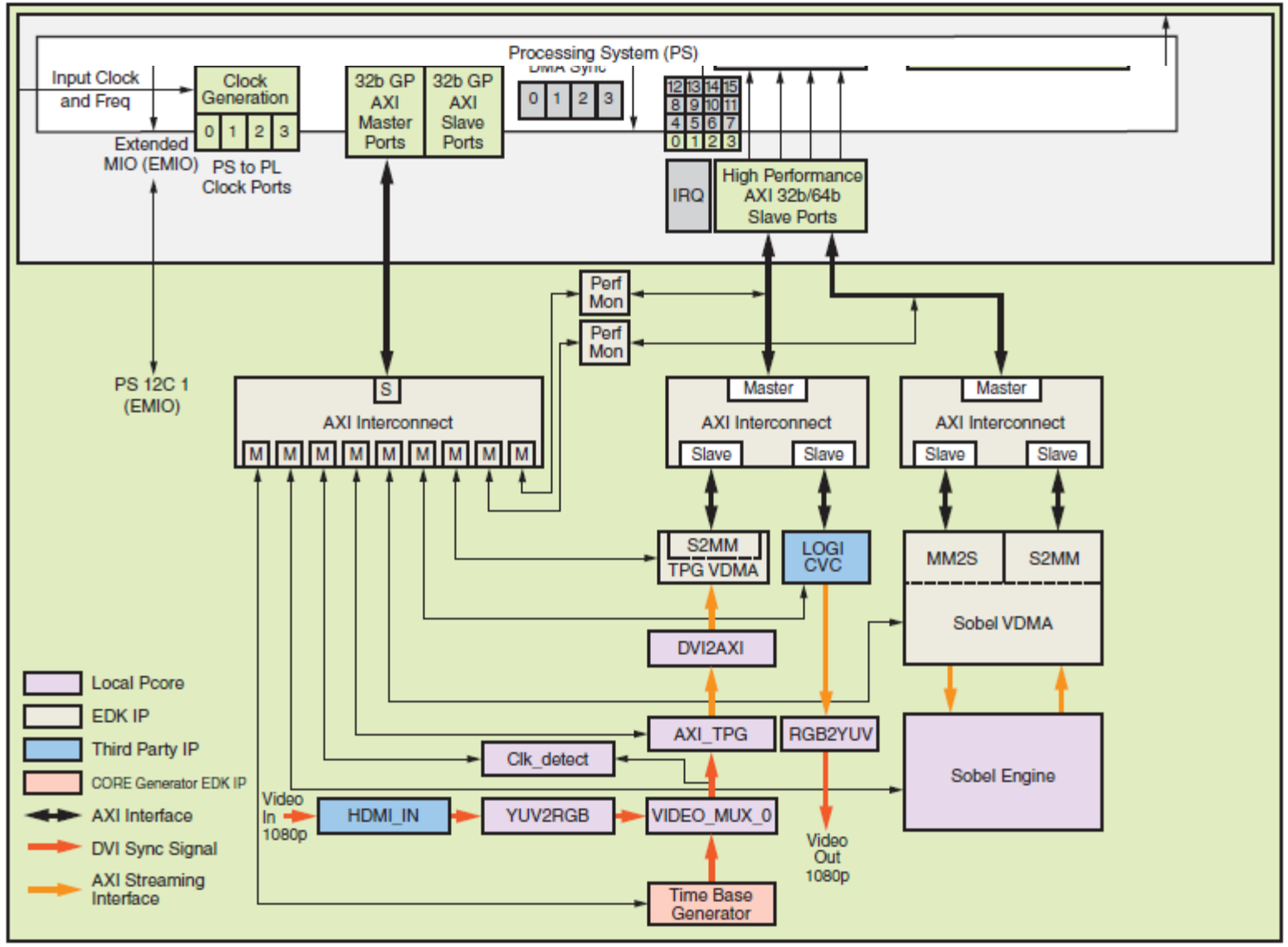
mLe missing link electronics

Motivation: System-on-Chip Design with Xilinx Zynq



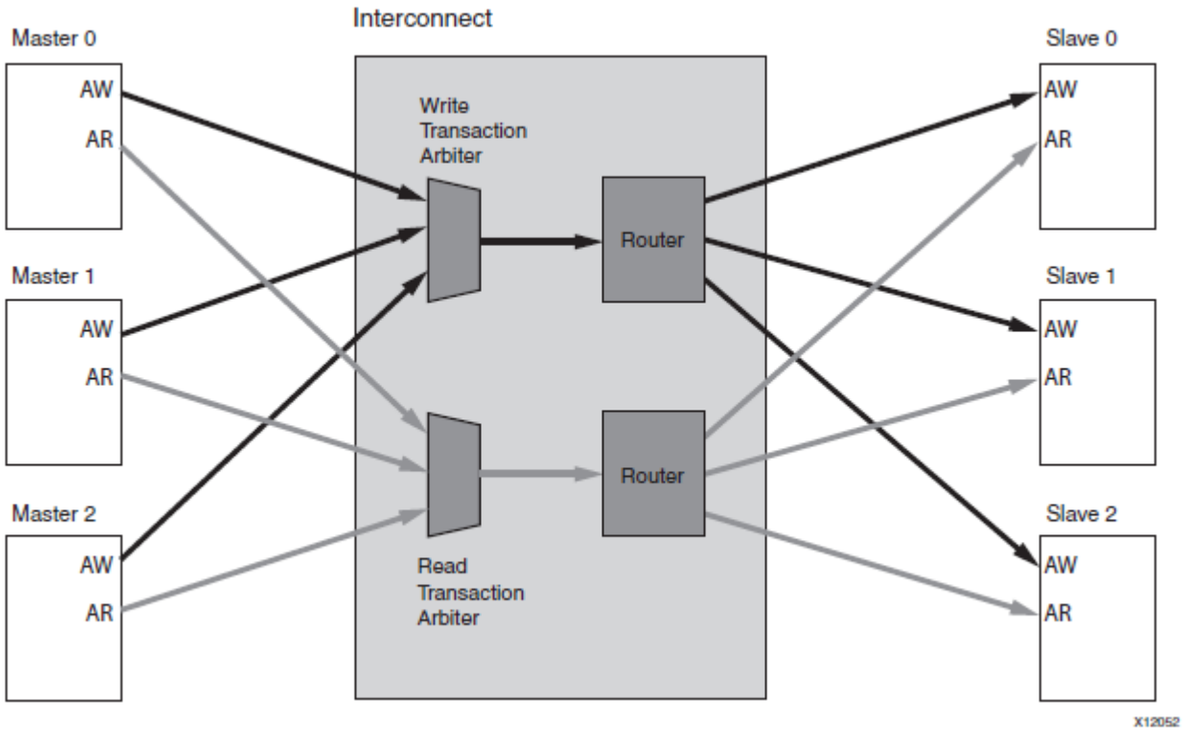
AXI4 to connect Programmable Logic (PL) blocks to the dual-core ARM A9 CPUs in the Processing System (PS)

Motivation: System-on-Chip Design with Xilinx Zynq



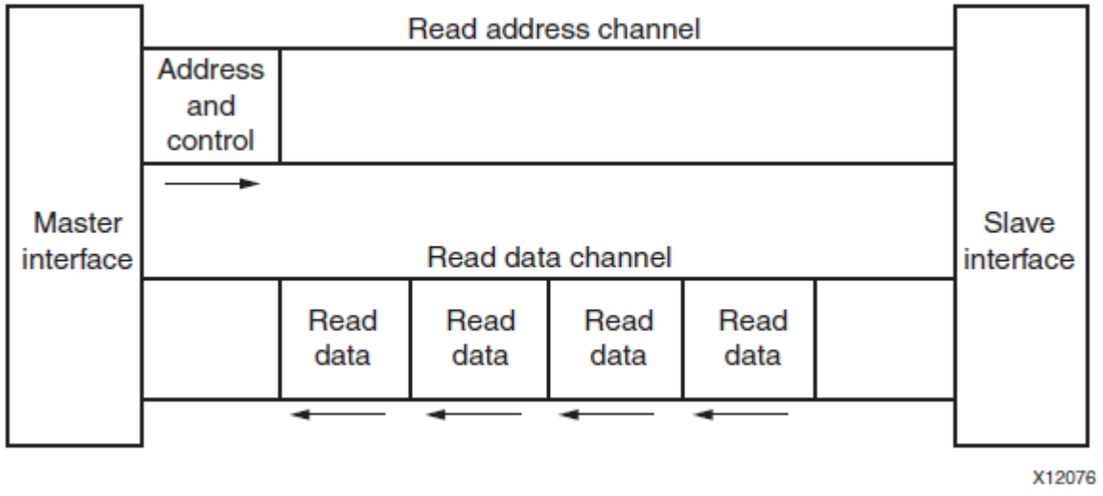
Backgrounder AXI4 Interconnect

"AXI4 Is Not a Bus!"

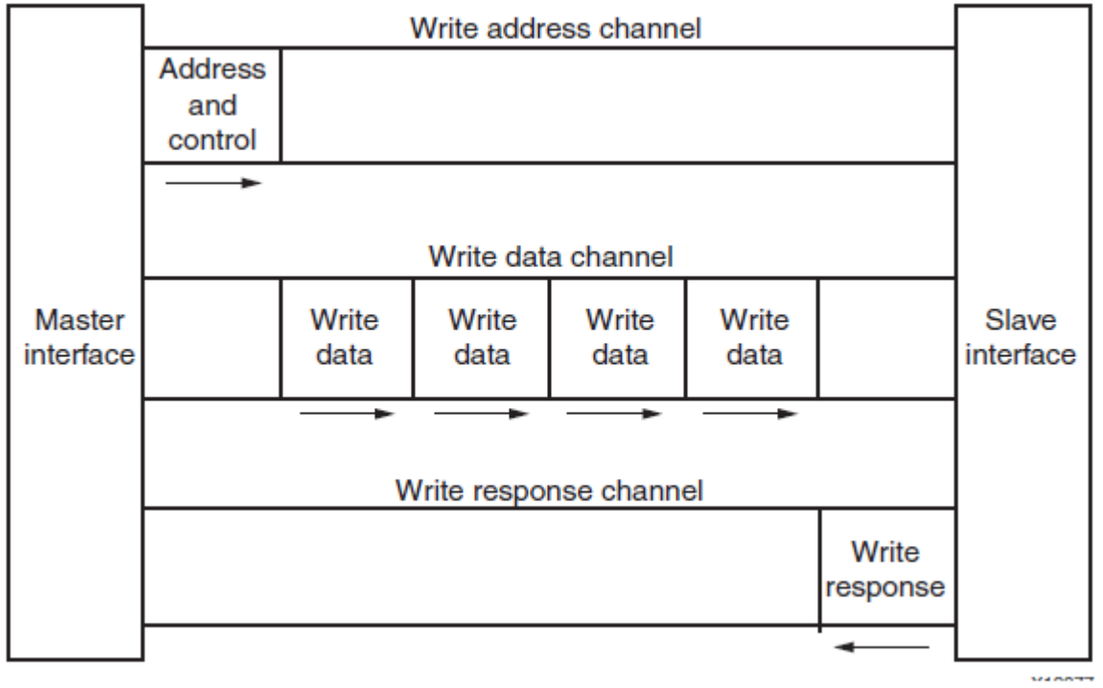


AXI4 Interconnect - Memory Mapped (Full AXI4 / AXI4 Lite)

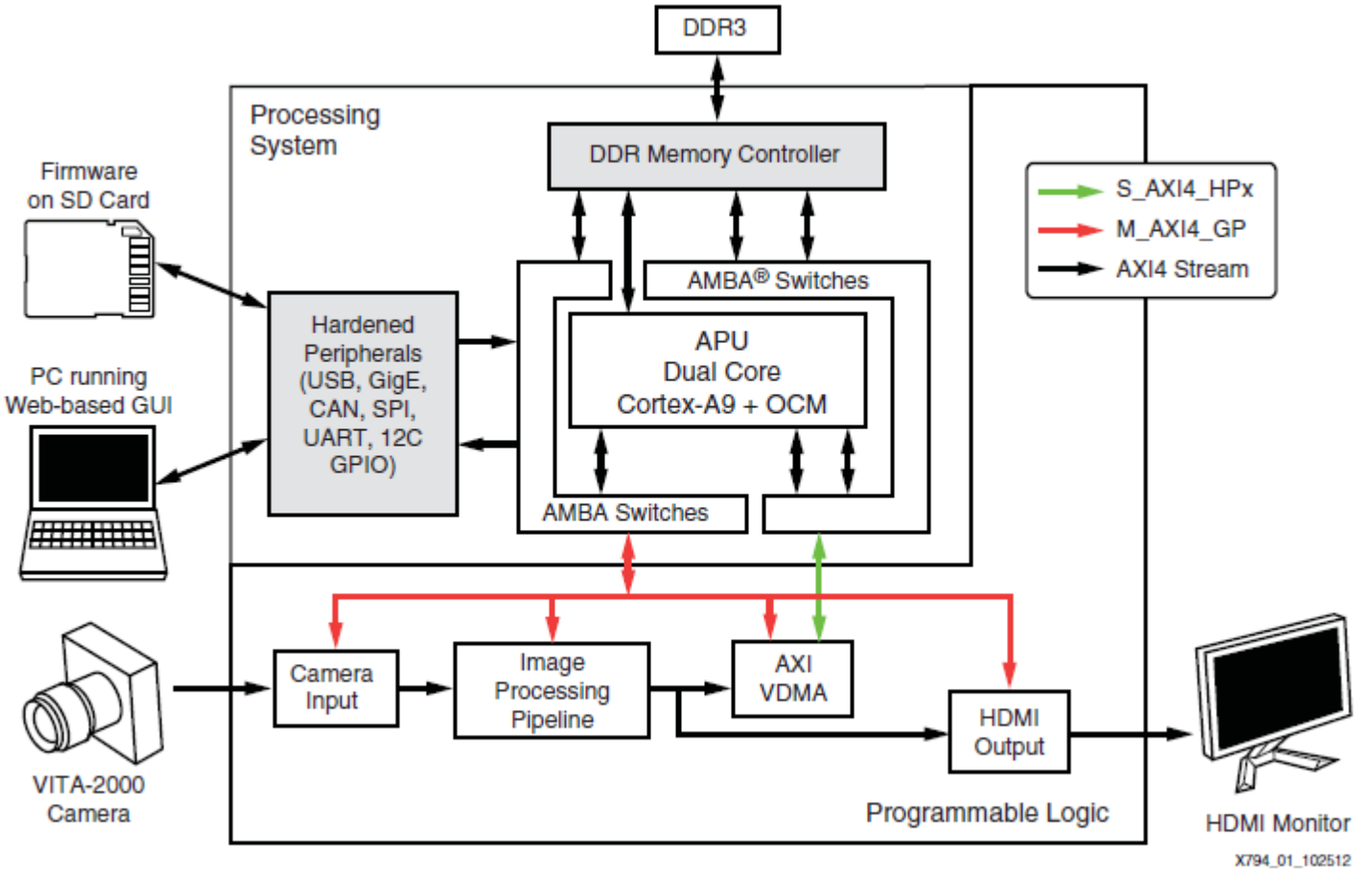
Read Access



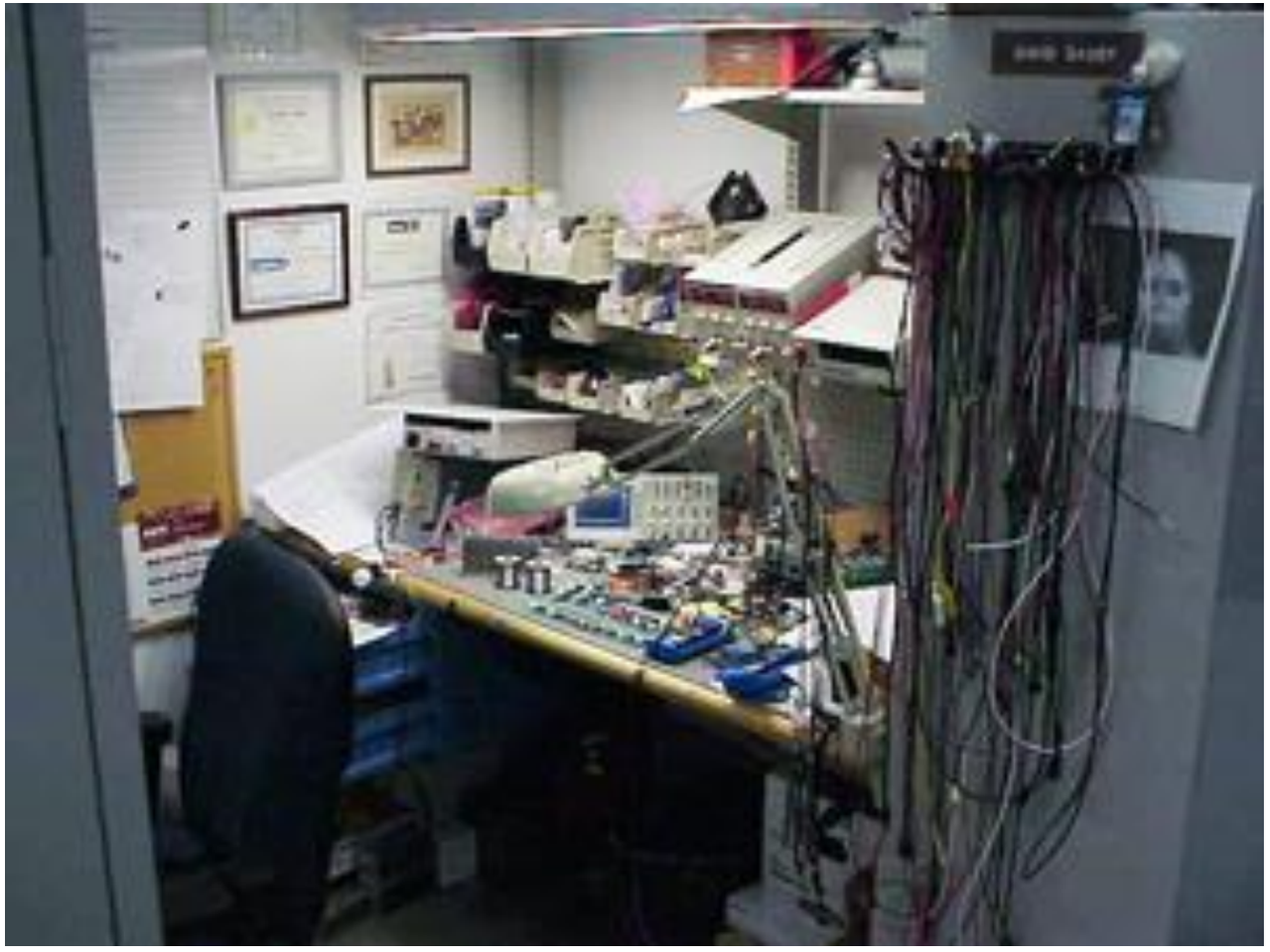
Write Access



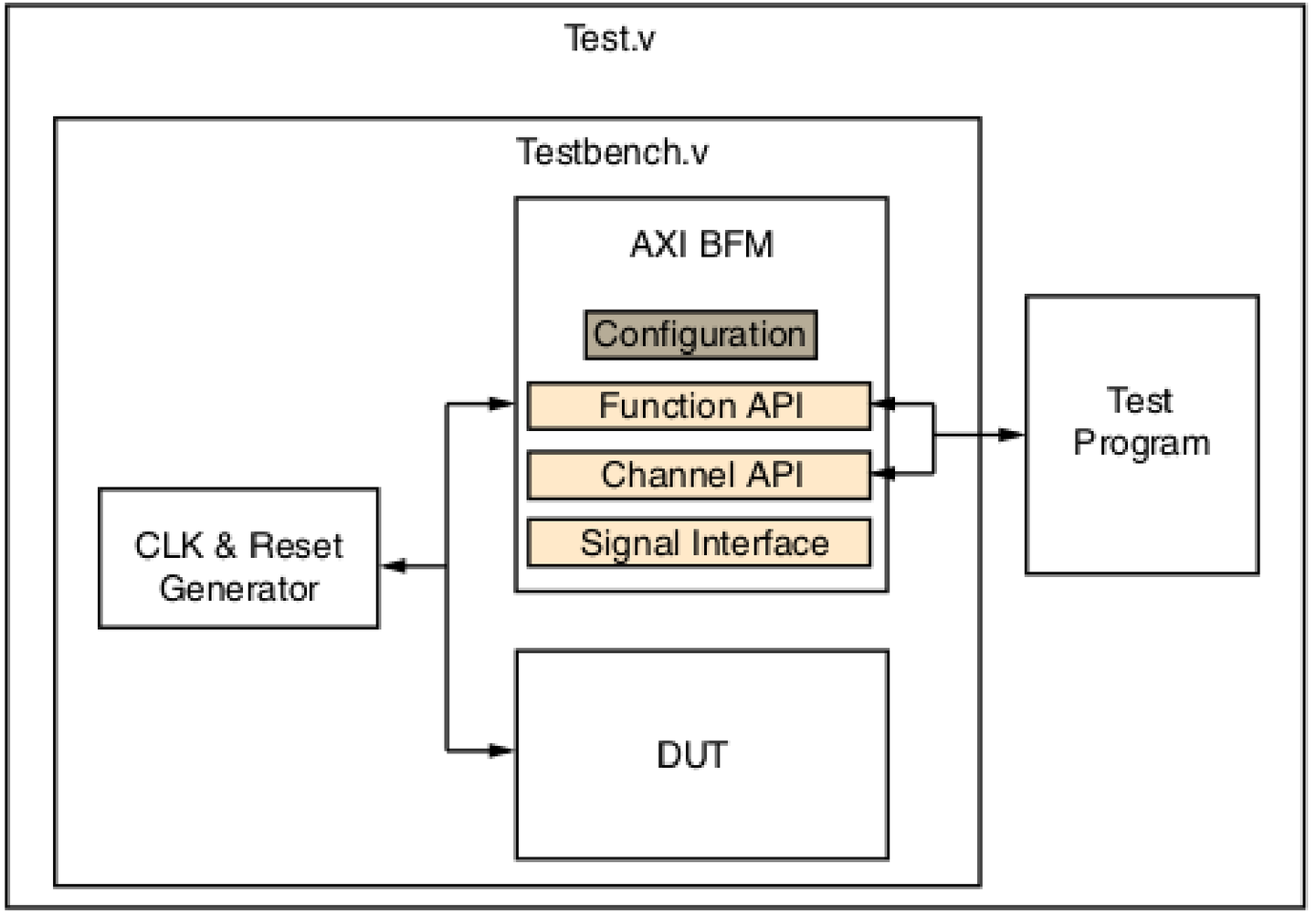
AXI4 Interconnect - Streaming



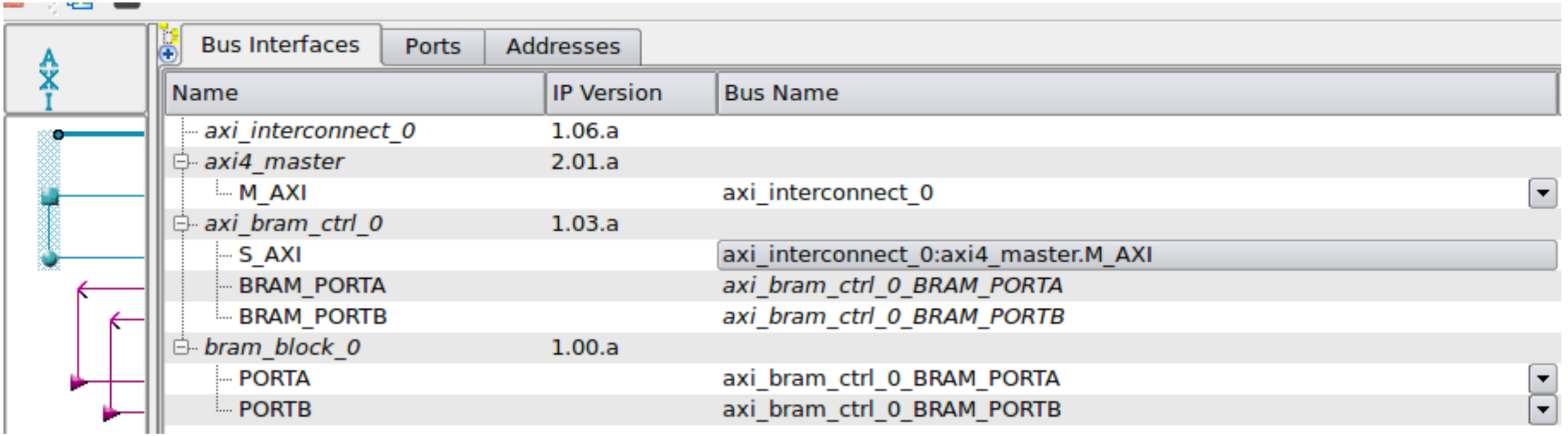
System-on-Chip Debugging



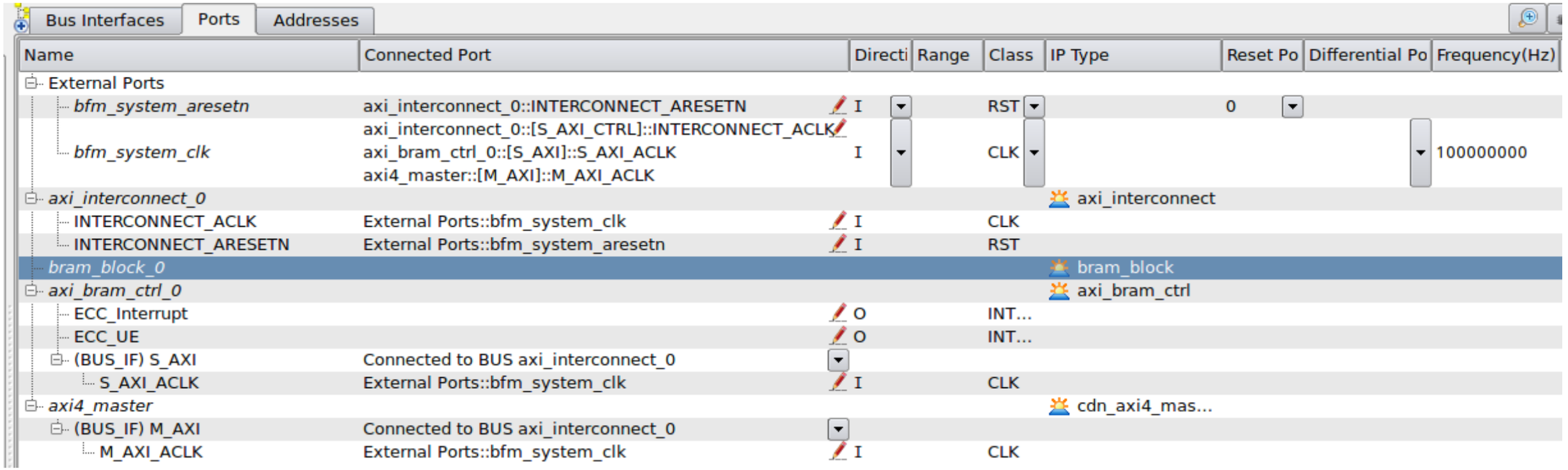
Test System for Bus Functional Models



AXI4 BFM in Xilinx XPS – Interface View



AXI4 BFM in Xilinx XPS – Port View



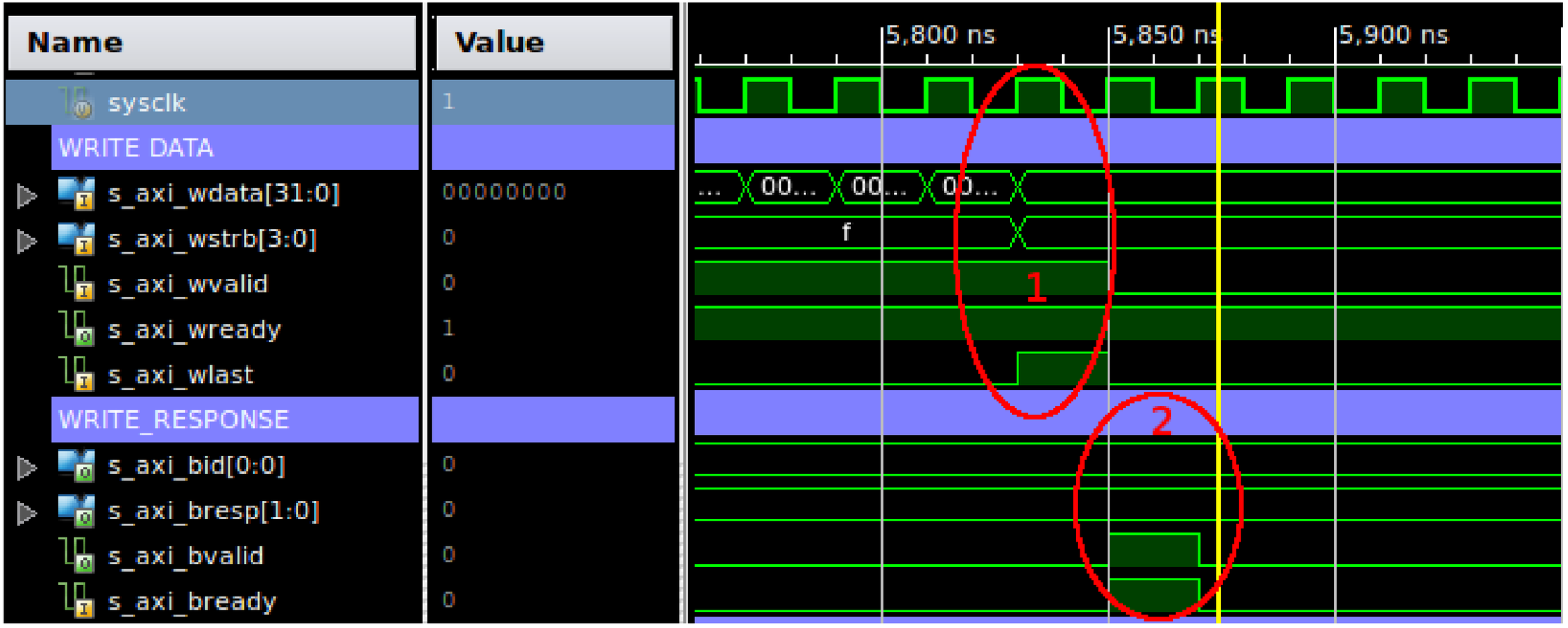
Bus Interfaces | Ports | Addresses

Name	Connected Port	Directi	Range	Class	IP Type	Reset Po	Differential Po	Frequency(Hz)
External Ports								
bfm_system_aresetn	axi_interconnect_0::INTERCONNECT_ARESETN	I		RST		0		
bfm_system_clk	axi_interconnect_0::[S_AXI_CTRL]::INTERCONNECT_ACLK axi_bram_ctrl_0::[S_AXI]::S_AXI_ACLK axi4_master::[M_AXI]::M_AXI_ACLK	I		CLK				100000000
axi_interconnect_0					axi_interconnect			
INTERCONNECT_ACLK	External Ports::bfm_system_clk	I		CLK				
INTERCONNECT_ARESETN	External Ports::bfm_system_aresetn	I		RST				
bram_block_0					bram_block			
axi_bram_ctrl_0					axi_bram_ctrl			
ECC_Interrupt		O		INT...				
ECC_UE		O		INT...				
(BUS_IF) S_AXI	Connected to BUS axi_interconnect_0							
S_AXI_ACLK	External Ports::bfm_system_clk	I		CLK				
axi4_master					cdn_axi4_mas...			
(BUS_IF) M_AXI	Connected to BUS axi_interconnect_0							
M_AXI_ACLK	External Ports::bfm_system_clk	I		CLK				

AXI4 BFM Instantiation

```
91      bfm_system.dut.axi4_master.axi4_master.cdn_axi4_master_bfm_inst.WRITE_BURST(
92              write_id,
93              write_address,
94              write_burstLength,
95              write_burstSize,
96              write_burstType,
97              write_lockType,
98              write_cacheType,
99              write_protectionType
```

AXI4 BFM Simulation



Additional Infos

- Xilinx ISE 14.2, or newer, with XPS version 14.2
- Xilinx ISim (version 14.2).
- License key for the AXI BFM (Part Number: DO-AXI-BFM).
- Xilinx DS824 - “AXI Bus Functional Models v2.1” (replaces Xilinx UG783)
- Xilinx DS768 - “LogiCORE IP AXI Interconect (v1.06.a)”
- AXI BFM example from http://www.missinglinkelectronics.com/devzone/axi-bfm

Kontaktinfo

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