Integration of Analog-Digital and Digital-Analog Converters into FPGA-Based Microcontrollers

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Abstract

Field-Programmable Gate-Arrays (FPGA) are well established for implementing programmable microcontrollers. A lesser known feature is their programmable digital I/O capabilities. Supporting Low-Voltage Differential Signaling (LVDS) at frequencies of many hundred MHz FPGA pins have become a viable option for quality analog I/O. Our approach utilizes the comparator of the LVDS I/O buffers inside the FPGA to implement a Delta-Sigma Modulator. A configurable, parameterized analog I/O architecture provides interesting trade-offs between precision, sample speed and FPGA resources.

1 Introduction

This paper presents a configurable, parameterized architecture for Analog-to-Digital converters (ADC) and Digital-to-Analog converters (DAC) based on so-called Delta-Sigma Modulators to directly connect analog channels to an FPGA. Combined with a fixed RC-filter at the I/O boundaries, this results in ADCs and DACs with sample ratios up to 500 kSamples/s and scalable resolutions exceeding 20 bits. Because of the noise-shaping effects of the over-sampling Delta-Sigma conversion one can achieve signal-to-noise ratios (SNR) above 60 dB.

The use of Delta-Sigma conversion to support analog channels in FPGA has been described, among others, in [3] or in [5]. Our approach extends these concepts and proposes a parameterizable architecture where operating coefficients can be adjusted towards an application's requirements in terms of sample rate and resolution.

Also, our ADC/DAC can be implemented as a 1st- or as a 2nd-order Delta-Sigma Modulator, depending on quality needs. An additional dithering block significantly enhances the stability over conventional approaches and avoids so-called Limit Cycles at the cost of very little additional noise. We present various experimental results of implementations in Altera Cyclone-IV FPGA devices that use very little resources and, therefore, can scale up to many analog I/O channels, each one suitable for reading sensor values or controlling actuators, for example. At the same time, noise and distortion ratios are more than adequate to also support high-quality audio sound.

We will first provide the theoretical background of parameterizable Delta-Sigma Modulators and go into the necessary details of LVDS for FPGA I/O. Then we will explain how we use Matlab/Simulink simulation models for selecting a proper parameter set to optimize the ADC/DAC towards a specific application. Finally, we will present quality analysis results of implementations using Altera Cyclone-IV FPGA devices.

2 Background

To understand the possibilities of our approach we will give the technical background of Delta-Sigma Modulation and how to implement this using the LVDS comparator inside an FPGA device.

Delta-Sigma Modulation

The Delta-Sigma Modulation is an advanced method of analog-to-digital and digital-to-analog conversion and is subject of current research [4]. The basic components of a 1st-order Delta-Sigma Modulator are described in Fig. 1. This Modulator comprises an integrator and an adder to sum up the differences between the input signal and a feedback signal.

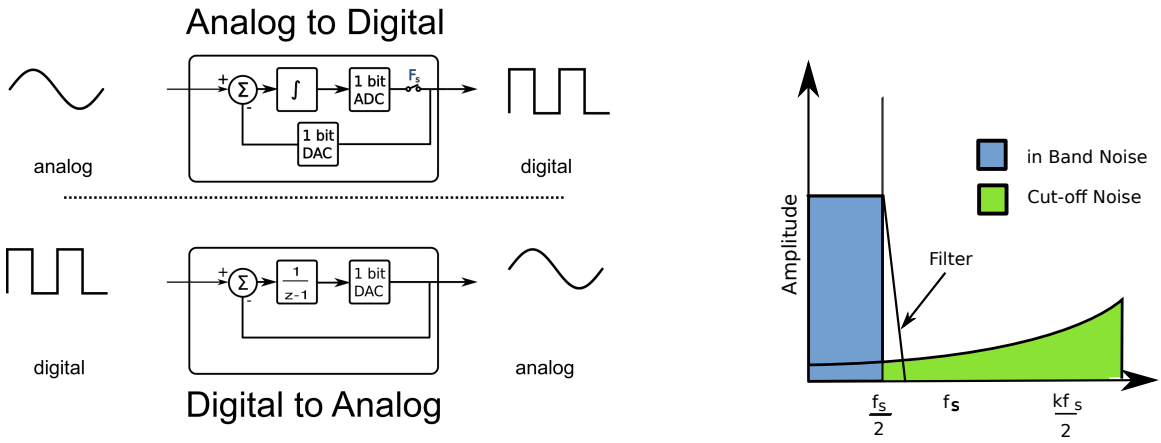

Figure 1: Delta-Sigma Modulator

Contrary to Nyquist rate converters – like the Flash Converter – the Delta-Sigma Modulation makes use of oversampling and noise shaping to enhance the results. The principles of oversampling and noise shaping are demonstrated in Fig. 1:Oversampling "spreads" the noise power over a wider spectrum. The out-of-band noise is then cut off by a lowpass filter which results in an overall noise reduction in the desired spectrum range.

To describe and to compare the quality of the I/O signals of the ADC/DAC, the Signal to Noise Ratio (SNR) is calculated, within a particular frequency band, e. g. for audio signals within 16 Hz - 20 kHz. Another often used value to describe the quality of signals is the Effective Number of Bits (ENOBs).

$$SNR = 10\log_{10}\frac{P_{Signal}}{P_{Noise}}dB; \qquad ENOB = \frac{SNR - 1.76}{6.02}$$

FPGA I/O Technology

FPGAs present an efficient and inexpensive alternative when it comes to implementing complete embedded systems along with important peripheral functions. The reconfigurable logic circuitry of an FPGA offers tremendous flexibility during the development phase and the product life cycle in addition to presenting a highly efficient solution for parallel applications. A lesser known feature is that the output pins of a digital FPGA also permit various analog applications:

First, FPGAs support the low-voltage TTL standard, which is suitable for many high speed connections. In our approach the 2.5 V LVTTL I/O with a current strength of 16 mA application is used for the ADC feedback and DAC 1-Bit output, for example [2]. A Level Shifter is necessary to drive higher voltages for the DAC output signal.

Secondly, modern FGPA device's I/O pins support LVDS. LVDS requires a fast, low noise comparator and can be used to transfer data at high speeds of 600 MHz or more at low power consumption. LVDS is a differential transmission standart. Fig. 2 shows the transmission characteristic of a LVDS transceiver pair. On the left hand side, the transmitter is shown with its' corresponding voltage ranges. On the right hand side, the receiver part of the LVDS transceiver is shown. A signal is transmitted by applying a voltage change to both differential transmission lines.

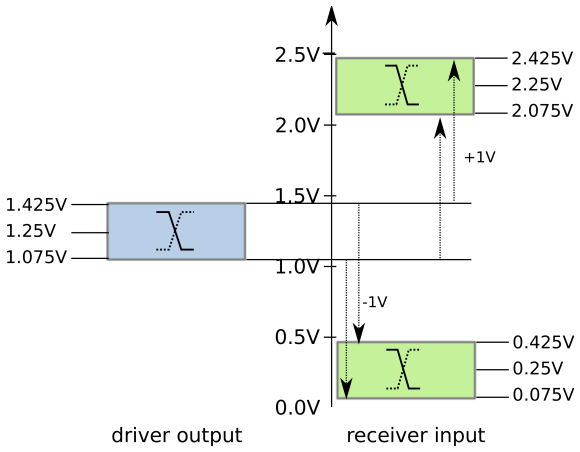

Figure 2: LVDS Common Mode Visualization

For resilience against transmission errors the LVDS standard calls for a wide input voltage range between 2.425 V and 0.075 V which defines the Common Mode. The voltage change during transmission, according to the LVDS specifications, must be at least 350 mV. However, the LVDS receivers inside the Altera Cyclone IV FPGA devices can sense a voltage difference of 100 mV [1]. This allows to utilize the LVDS receiver as a sensitive, high-speed 1 bit ADC.

3 ADC/DAC Parameterization

To implement ADC/DAC channels we use a parameterized Delta-Sigma Modulator which allows to trade off between quality of results and FPGA resources. Matlab/Simulink simulation models, one for the ADC, and another one for the DAC, facilitate finding the best parameter set, depending on the application.

ADC Simulation Model

This simulation model is to determine the parameters of the Delta-Sigma Modulator such as the time constant of the RC-integrator and the sample rate [6]. The Matlab/Simulink model is shown in Fig. 3.

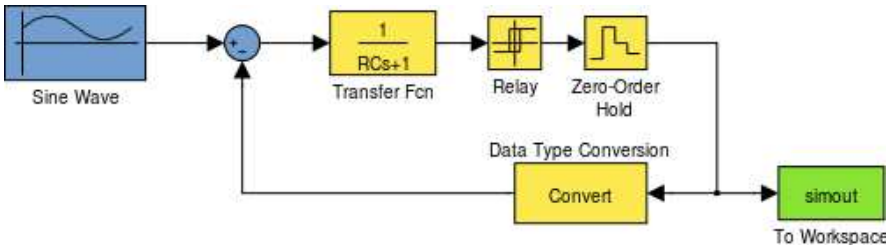

Figure 3: ADC Simulation Model for Parameterization

This model was executed for different parameter combinations (RC time constants and oversampling ratios) and the resulting SNR values were plotted in a heatmap. An exemplary heatmap is shown in Fig. 4 which provides values for the lowpass as well as the oversampling ratio and RC time constants for a desired SNR value.

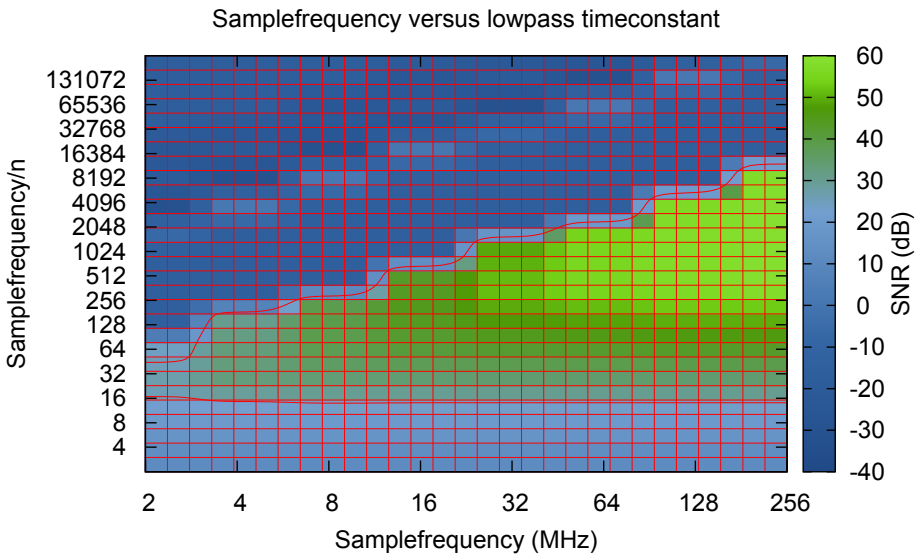

Figure 4: ADC Parameter Analysis Results

DAC Simulation Model

Fig. 5 shows the Matlab/Simulink model for the Delta-Sigma Modulator used as a DAC. This model is for a 2nd-order Delta-Sigma Modulator with a 1-bit quantization output and feedback coefficients a_1, a_2 and the input coefficients b_1 and b_2 [7]. For audio analysis a sine wave generates input signals between 1 Hz - 20 kHz at sampling frequencies of 44.1, 48, 96 and 192 kHz. The model can be configured for 14, 16 and 20 bit input word lengths. The Delta-Sigma Modulator (colored in yellow) itself has a configurable oversampling ratio $OSR = \frac{f_{clock}}{f_{sample}}$ of 32, 64, 128, 256 and 512.

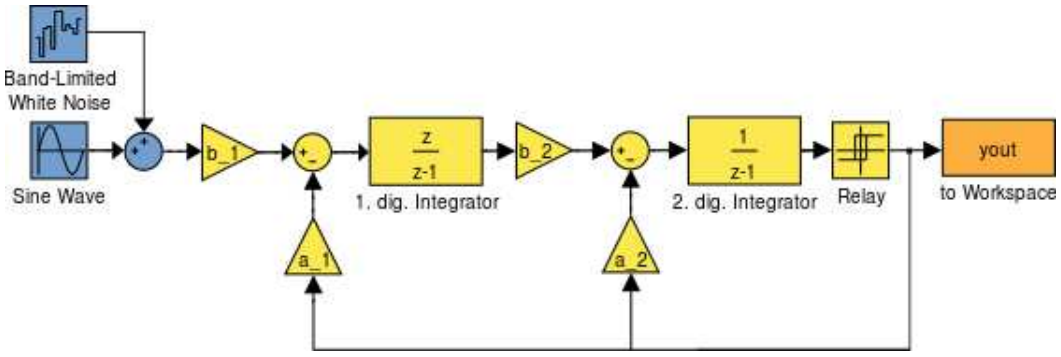

Figure 5: DAC Simulation Model for Parameterization

Fig. 6 shows the simulated SNR of the 2nd-order Delta-Sigma Modulator with different feedback and input coefficients. To reduce the search space, the cofficients a_1 and b_1 (a_2 and b_2, resp.) have the same value. The best possible SNR is 85 dB, achieved at an OSR of 128 for an input signal of 1kHz at sample frequency of 48 kHz. This translates to approximately 14 ENOB.

4 Implementation and Results

For practical signal analysis we implemented our approach using Terasics' DE2-115 INK board featuring an Altera Cyclone-IV FPGA device, EP4CE115. The Cyclone-IV is a current generation low-cost FPGA, built in a 60 nm process with high-k dielectic. It offers many high-speed LVDS

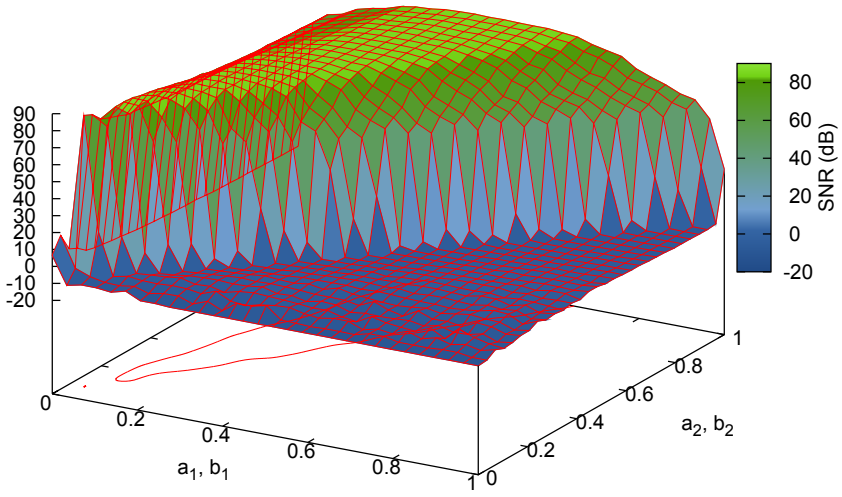

Figure 6: DAC Parameter Analysis Results

receivers and fast I/O switching capabilities. The EP4CE115 device has 114k Logic Elements (LE), 4 PLLs and 528 single-ended user I/O and 230 differential I/O channels.

Our configurable analog I/O architecture is shown in Fig. 7. It comprises an ADC component as well as a DAC component inside a configurable ADC/DAC slice. The ADC requires two external resistors and one external capacitor for the analog integrator. The DAC component requires one external resistor and one external capacitor as an analog lowpass filter to interpolate the DAC output bitstream. As described above, the analog filters are connected via LVTTL output; built-in LVDS receivers are used to provide a 1 bit ADC for the Delta-Sigma Modulator.

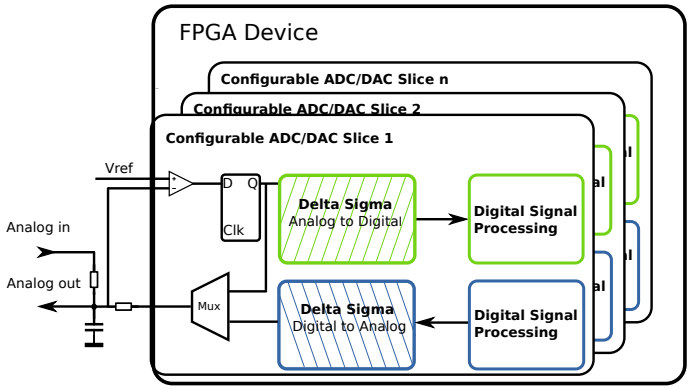

Figure 7: Configurable ADC/DAC Architecture

To test and measure the analog quality and to validate the parameters obtained during simulation, we used the setup of Fig. 8. Altera's built-in Logic Analyzer, SignalTap, was used to receive the results of the ADC. An Agilent Spectrum Analyzer was used to measure the analog output quality of the DAC.

ADC Results Discussion

The test and measurement setup validates our 1st-order Delta-Sigma ADC. For the ADC part the SNR was measured using various sample rates and different filters for digital signal post-processing. We experimented with a CIC filter followed by a FIR filter (as the literature [3] suggested), and with a moving average filter with a decimation (DEC) module. The results are shown in Fig. 9:

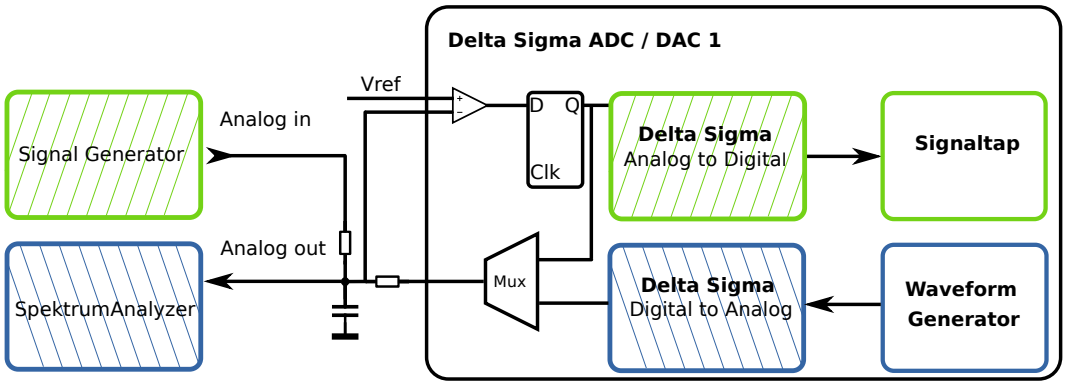

Figure 8: ADC/DAC Test Setup

The DEC filter not only delivers a better signal quality but is also more resource efficient.

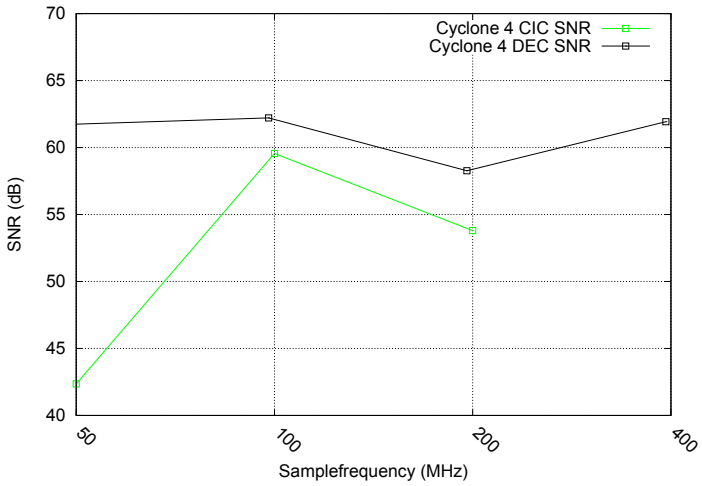

Figure 9: ADC Quality Comparison

The results show that the Delta-Sigma Modulation offers SNR values of above 60 dB which equals about 10 bits ENOB by only using two resistors and one capacitor. It also shows the need for matching filters as the comparison between CIC and moving Average filter shows. Due to the high bit gain of the CIC filter it has a high resource usage which is shown in Table 1.

DAC Results Discussion

The test and measurement setup of Fig. 8 also validates our 1st-order Delta-Sigma DAC with and without dithering and compares it against a 2nd-order Delta-Sigma Modulator. This results in three different designs with different converter quality and resource requirements.

Fig. 10 compares these three DAC alternatives for different oversample frequencies up to 10MHz. Obviously, the 1st-order Delta-Sigma Modulator without dithering delivers better SNR as the 1st-order design with dithering, however, dithering becomes important for audio applications. By adding extra noise – generated via a 8-Bit Linear Feedback Shift Register (LFSR) – the 1st-order Delta-Sigma Modulator delivers a less distorted sound. The best result is achieved with the 2nd-order design, ultimately giving SNR of 80 dB, or an ENOB of 13 bits. The noise shaping and oversampling effects of a 2nd-order Delta-Sigma Modulator clearly are superior.

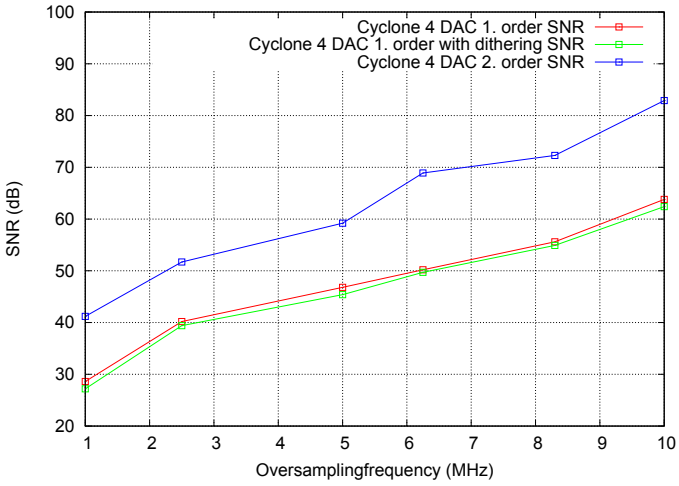

Figure 10: DAC Quality Comparison

Fig. 11 shows the spectrum of 1 kHz signal for the ADC, and for the DAC, resp. The spectrum of the DAC was measured with a Spectrum Analyzer, while the output of the ADC was measured with SignalTab.

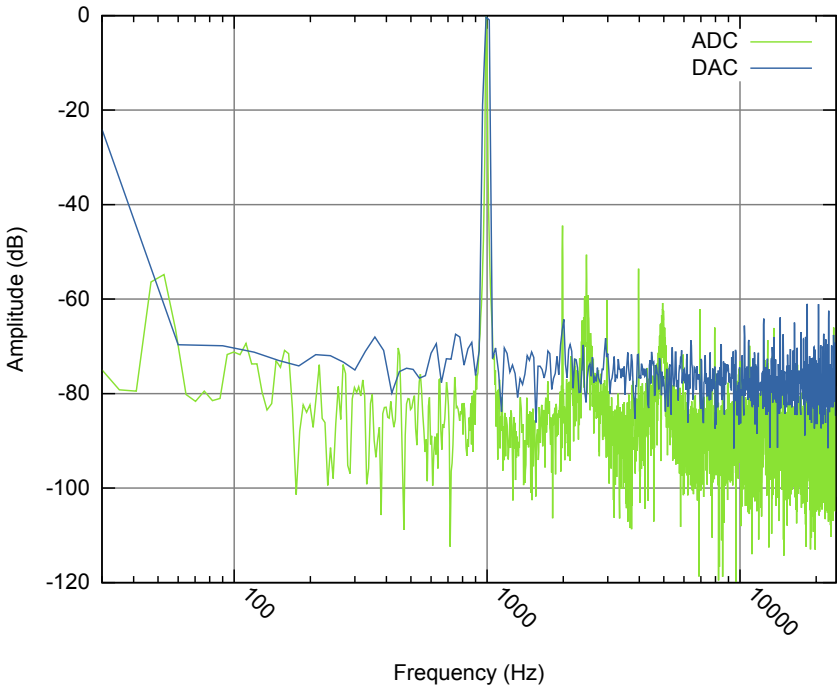

Figure 11: ADC/DAC Signal Spectrum

FPGA Resources

The resource requirements for the different ADC/DAC alternatives are shown in Table 1. The ADC version with the DEC filter clearly uses significantly less hardware than the version implementing a CIC filter.

For the DAC, we see an increase of resources by adding the dithering block which reduces the distortion of the 1st-order Delta-Sigma Modulator. The 2nd-order Delta-Sigma Modulator DAC,

obviously, needs more resources than the 1st-order version. However, each ADC/DAC slice is tiny when compared to the resources available in the EP4CE115 device: 114,480 Logic Elements (LE), 3,888 M9K memory blocks, 588 user I/Os.

Design	Usage LEs	Usage M9K
ADC CIC	4000	0
ADC DEC	124	1
DAC 1st-order	23	0
DAC 1st-order dithered	42	0
DAC 2nd-order	87	0

Table 1: ADC/DAC Resource Cpomparison

This makes it possible to have many ADC and DAC channels on one FPGA, literally only limited by the pin count of the devices and the resource requirements of the digital logic for further data processing. For the Altera INK system, it should be possible to have many tens of analog channels.

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