Fully Integrated FPGA-based configurable Motor Control

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Abstract

Field programmable gate arrays (FPGA) provide outstanding hardware design flexibility. This enables to implement a fully customizable peripheral set and also to meet increasing performance requirements via multi-core and hardware acceleration techniques. Another key benefit is the protection against hardware obsolescence. Lesser known features are certain analog-to-digital conversion (ADC) and digital-to-analog conversion (DAC) capabilities of FPGAs. This presentation describes how we used these features to implement a fully integrated FPGA-based configurable controller for brushless DC motors. Our closed-loop controller comprises compact Sigma Delta Modulators for ADC as well as DAC, implemented inside the FPGA. Based on that, our proposal features shoot-through prevention plus a soft motor startup by measuring the electro-magnetic motor feedback. This technique reduces PCB and parts costs and gives extra I/O flexibility: Designers can add large numbers of analog I/Os to their embedded systems!

1 Introduction

Field-Programmable Gate-Arrays (FPGA) provide additional levels of flexibility throughout the design phase and the product life-cycle. They can implement parallel signal processing, support a variety of I/O connectivity, and can counter parts obsolescence. When used as a companion solution to general purpose processing, these so-called Configurable Systems apply to monitoring, control and supervisory of physical systems, an aspect which sometimes is called Cyber-Physical Systems [1]. Many such applications, like battery monitoring in electrical vehicles, require a multitude of analog I/O at reasonable precision.

Delta Sigma Modulators with their oversampling and noise-shaping effects can be used to integrate Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC) inside FPGAs [2, 3].

DAC inside FPGAs are quite robust and deliver good signal-to-noise rations (SNR) above 80 dB leading to reasonable precision of 12 bits and more. The ADC side, however, utilizes the FPGA's Low-Voltage Differential Signaling (LVDS) pins and, therefore, requires more diligent parameterization to obtain reasonable precision. One interesting field of application for this method is in areas, where multiple Analog-to-Digital channels are needed. We will provide an examplary implementation utilizing a brush-less DC (BLDC) motor. This motor has an electrical commutation, therefore, multiple ADC channels for acquiring the current motor position are needed. This example features a standard 3 phase BLDC, as this type of motor is used in applications ranging from fans cooling PCs to the growing electro-mobility sector. As these sectors are cost-sensitive, a sensor-less implementation using the back-EMF was chosen.

2 Background

Today's FPGA devices not only deliver programmable logic but also very flexible programmable I/O connectivity. This includes Low Voltage TTL (LVTTL) as well as Low Voltage Differential Signaling (LVDS) capabilities. The latter comes as pin pairs with a built-in comparator for handling the voltage difference between to two pins which can be used as a digital 1 bit comparator. However, special attention must be given to the so-called "common mode" where a 350 mV amplitude delta is needed for a detection. LVDS pins either feature an implicit (in our case) or require an explicit R=100 Ohm resistor, which converts the LVDS standardized current signal into a voltage locally at the LVDS receiver. The receiver works then around a common mode signal of 1.25 V with differential input signals in the 200 mV range - but at speeds of above 1 GHz. When going to lower sample speeds, the LVDS receiver can also be used as a comparator, operating on much smaller voltage input differences. Also, most FPGA LVDS receivers have a quite flexible common mode voltage of the receiver, making them even more suitable for this application.

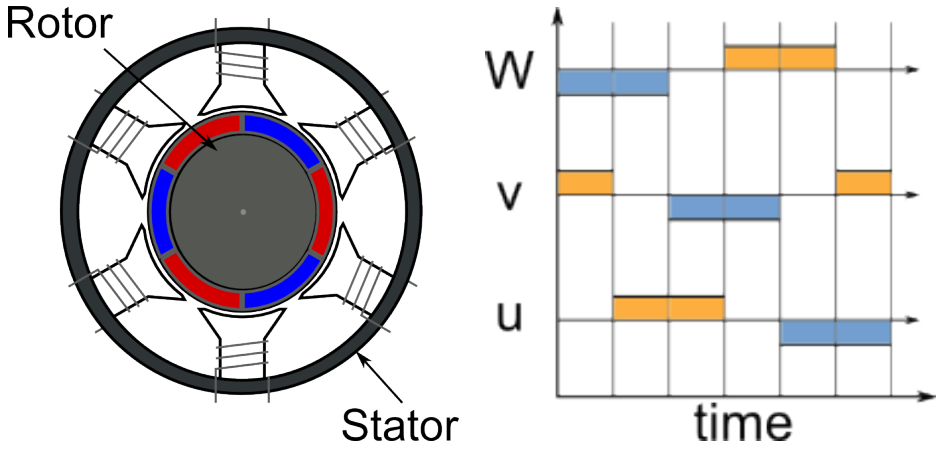
2.1 Delta Sigma Modulation

The Delta Sigma Modulation while subject of ongoing of research, has found its way into many applications. A Delta Sigma Modulator has the noise shaping ability as stated in [4], which means the noise of the 1 bit ADC is high-pass filtered, and the signal is low-pass filtered. This produces a possible signal to noise ratio gain of 9 dB per octave as stated in [5] which allows to achieve high Signal-to-Noise ratios (SNR) and a wide Spurious-Free-Dynamic-Range (SFDR). When used for DAC Delta Sigma Modulators show very robust behavior and - once properly parametrized can deliver reasonable precision of 12 bits and more. [2] describes how to utilize the functionality of LVDS pins in FPGAs to implement ADC. This implementation, however, implements a Delta Modulator leaving out the advantageous noise-shaping effects. This left room for improvement. The circuit is extended by an integrator component to implement a 1st-order Delta Sigma Modulator. Also an important optimization is that a less complex moving-average filter – replacing the Cascaded-Integrator-Comb (CIC) filter – was sufficient for good SNR. This significantly reduces the amount of resources needed in FPGAs and opens-up the possibility to integrate 10s, if not 100s, of ADC inside a single FPGA device [6, 7].

2.2 Brushless DC Motors

Brushless DC Motors (BLDC) are electronically commutated motors driven by direct-current (DC) electricity, and thus do not rely on mechanical commutators and brushes. Their use of rotating magnets instead of a exciter coil is a key to their higher efficiency, as no energy is used for the exciter. With the introduction of rare-earth magnets which have a high magnetic flux density, these motors have gained a boost in torque. The drawback of this is the need for an electronic commutation.

There are two mechanical types of BLDC motors, the standard configuration (inrunner), and the outrunner configuration. In the inrunner configuration, the permanent magnets are inside the rotor, and three stator windings surround the rotor. In the Outrunner configuration, the stator coils are at the center of the motor, and the permanent magnets of the rotor are build around these. Ourunners usually have a higher torque output than Inrunners at low revolutions per minute. Fig. 1(a) shows the buildup of a typical Inrunner BLDC motor.



(a) BLDC motor (b) Phase Diagram

Figure 1: Brushless DC Motor Functioning

BLDC motors usually have three different phases, which have to be driven independently. This is usually done by using a 3 phased bridge circuit. The phase diagram principle for driving the BLDC motors is shown in Fig. 1(b). It shows how the different phases have to be high or low depending on the position of the rotor. To acquire the position there is the possibility to use an external sensor, which is usually done using three HALL sensors. Another method is to use the back-EMF of the motor to calculate the position.

The back-EMF is a counter-electromotive force which is generated by the rotation of the motor, and can be used to obtain the current position of the rotor. In a BLDC motor, there are always two phases which conduct and one phase is floating. This is the phase were the back-EMF can be measured against the motor neutral point, or a virtual neutral point. The more common approach is to use zero crossing detection using a comparator, but using the Delta-Sigma ADC, a Third Harmonic detection can be implemented which gives more exact rotor position information.

3 Soft ADC for FPGAs

Foundation of our analysis was the implementation of the passive 1st-order Delta Sigma Modulator ADC, shown Fig. 2. Here, the LVDS pins via the feedback effectively implement a 1-bit comparator while the loop-filter is realized with a passive RC-low-pass.

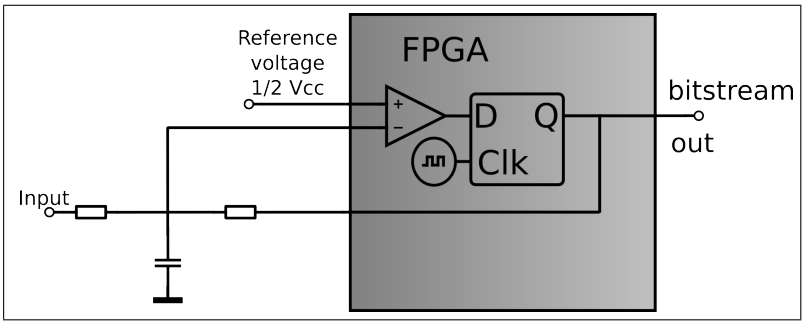


Figure 2: First-order FPGA-based Delta Sigma Modulator

Obviously, the "analog" behavior of an LVDS pin - such as hysteresis, finite amplitude decision time, metastability, etc - cannot be ignored as they will determine the possible SNR of the ADC. Therefore, we perform a systematic analysis of the DSM of Fig. 2 using simulation model the highest level of accuracy, the transistor or SPICE level. The anticipated effect of these non-linearities is an effect as shown in Fig. 3, where the effect of the non-linear adder (i. e. the two external resistors) and the LVDS-comparator provide one sweet spot where good results, i. e. high Effective Number Of Bits (ENOB), can be achieved.

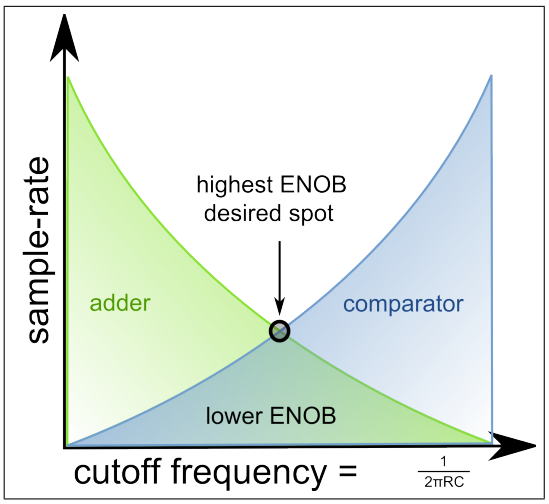


Figure 3: Dependencies for good SNR

Finally, the SPICE model provides the most accuracy: The low-pass can be modeled as a resistor-capacitor pair, the comparator matches a linear op-amp model, and the LVTTL pin was modeled in accordance closer to physical pin implementations. While this model delivers the highest accuracy, it unfortunately requires the most compute time to simulate. One limitation in accuracy was, that the limitation in accuracy is that only a straight forward LVDS model was used. Obviously the SPICE level model can be enhanced by using SPICE models from the FPGA vendors which was done in cooperation with Altera and resulted in a model which is reasonably accurate. This last model delivers a signal-to-interface ratio including noise and distortion (SINAD) of 52$\tilde{\text{d}}$B in a signal band from zero to 20$\tilde{\text{k}}$Hz and an input signal of 1 kHz. The Fourier spectra of this model can be seen in Fig 4.

A multitude of these simulations are executed to find combinations of the external R C setting and the sample rate where the need of both the adder and the comparator are satisfied and, as a result, best conversion results will be achieved.

To verify the measurements, the whole Delta Sigma Modulator based ADC was measured with different parameters. The measurements showed a resulting SINAD of 52$\tilde{\text{d}}$B and an SNR of 72 dB.

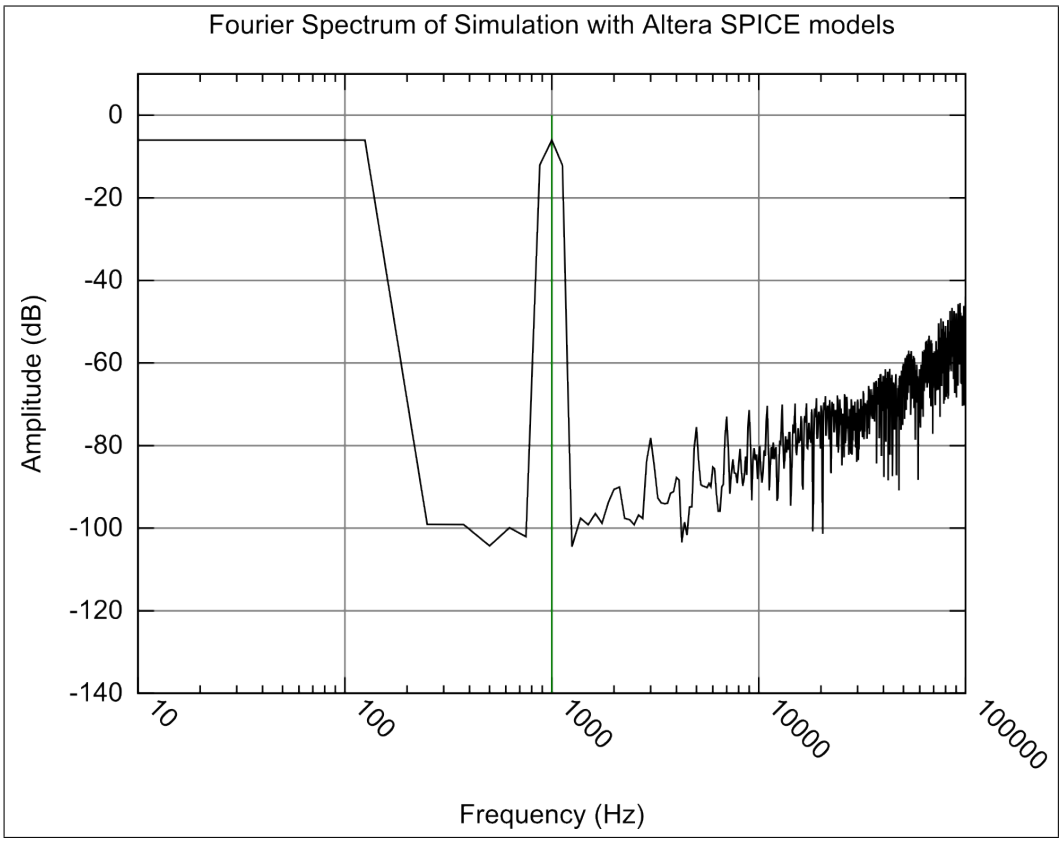


Figure 4: Spice model Fourier spectra with 1 kHz Input

4 FPGA-Based BLDC Motor Control

This chapter shows the actual implementation of the Delta Sigma ADC, as well as a possible implementation, using the ADC channels to control a BLDC motor. Fig 5 shows the implementation on an FPGA including the passive external circuitry. The difference to the previous implementation is the use of a low-pass and a decimation filter to obtain results compatible to an FPGA-based micro-controller. For our exemplary implementation we have used the Nios-II CPU [8] which is available as a soft IP core and can be integrated inside the FPGA plus extra peripherals to form a customizable micro-controller. For the low-pass filter, a resource-efficient moving average filter was chosen, as the normally-used CIC filter is not resource-efficient at high oversampling ratios. This ADC was inserted as a soft IP core into the FPGA design. The brush-less controller consists of different

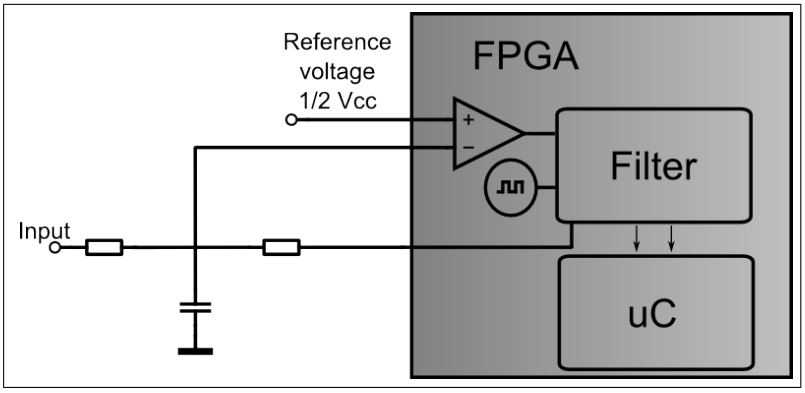


Figure 5: FPGA based ADC

modules as shown in Fig. 6. The motor control is done using 3 output modules with a shoot-through prevention each of which connects to the three phase H-bridge which drives the motor. Three Delta-Sigma ADC channels

with specialized protection circuits sample the back-EMF the corresponding back-EMF from the motor. From

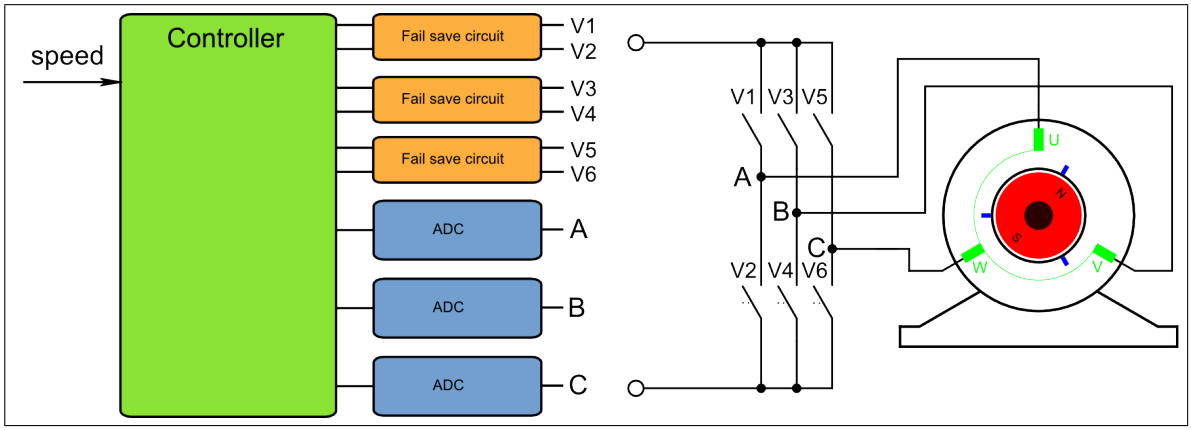


Figure 6: Brushless Controller

this data, the position of the motor is extrapolated. Connected to these input and output modules is the actual control module which calculates from the back-EMF, the current outputs and the desired speed of the motor the next output of the H-bridge. This modular design also makes the controller adaptable to different motor types and sizes.

5 Conclusion

It can clearly be seen, that the Delta Sigma ADC conversion scheme shows conversion results suitable for many applications where multiple simultaneous ADC channels are needed. The measurement show, that a proper parameterization is needed to obtain reliable and stable results. Because it is possible to adjust the input voltage via changing the external resistors, this ADC offers many possibilities to reduce the number of parts on your printed circuit board. This offers cost-efficiency and on top reduces the risk of part-failure. To sum it all up, this approach delivers a flexible and cost-effective approach for implementing a motor controller inside an FPGA using only minimal external circuits.

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